The Dissertation Committee for Matthias Kraatz
certifies that this is the approved version of the following dissertation:

Studying the Effect of Cu Microstructure on Electromigration Reliability using Statistical Simulation

Committee:

Paul S. Ho, Supervisor

Li Shi

Dean P. Neikirk

Desiderio Kovar

Ehrenfried Zschech

Andreas Knorr

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by

Matthias Kraatz, Dipl.-Phys.

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Dedicated to my parents.

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Studying the Effect of Cu Microstructure on Electromigration Reliability using Statistical Simulation

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Electromigration (EM) describes the mass transport in a metal driven by the momentum transfer from electron scattering with metal ions. This can develop into a degradation process due to void growth for on-chip interconnects when subjected to high electric current densities and eventual interconnect line failure. The mass transport occurs in decreasing order of magnitude along interfaces grain boundaries and in bulk. The diffusivities along interfaces and grain boundaries are determined by crystallographic orientation. Diffusion discontinuities can create flux divergent sites that control void growth kinetics and failure characteristics. Most of the earlier studies of EM modeling have assumed an averaged diffusivity measured across the underlying crystallographic microstructure. The objective of this thesis is to study the effect of microstructure on EM reliability by modeling of the diffusivity corresponding to grain orientation at the interface and to project the EM lifetime and the standard deviation (sigma) of the failure statistics. The simulation consists of two parts. First, the microstructure is generated using a Monte Carlo algorithm based on the Potts model. In the second stage, the void formation and growth induced by electromigration is modeled until a maximum time elapsed. During the void growth, the electrical resistance is monitored to search for EM failure subjected to a 400% (5 times the initial value) resistance increase failure criterion. The simulated electromigration lifetimes were found to follow a log-normal distribution. The computations were carried out on a parallel computer, simulating a population of 100 interconnect segments with random microstructure configurations. In this way, the 100 interconnect segments form the basis for statistical analysis of a special simulation run. Simulation runs were carried out with microstructures varying over a range of grain sizes and diffusivity for the top interface. In the simulation, four cases were studied and compared to results from EM experiments. These four cases were large and small grains combined with slow and fast diffusing top interfaces. Results from the simulation revealed a consistent trend in that large grains prolong the electromigration lifetime, especially for the case of a slow diffusing top interface. This trend is also consistent with the experimental results where the lifetime was found to increase in the order of small grain/fast interface, large grain/fast interface, small grain/slow interface and large grain/slow interface. The overall agreement, however, is only qualitative. For instance, the EM experiment showed a lifetime improvement of more than 100 fold whereas the simulation only showed an improvement of 6 fold from fast to slow interface for large grains.

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Chapter 1

Introduction

Copper damascene interconnects have been used in leading-edge microelectronic products for more than two decades. Electromigration is one of the most critical reliability concerns for copper interconnects. This effect is caused by directed atom transport under the influence of an electric potential gradient where thermally diffusing atoms interact with an electric field and current causing random diffusion to become biased motion. Net electromigration-drifted Cu atoms have been found in the direction of electron flow [3]. This transport of mass could ultimately cause catastrophic failure in on-chip interconnects by the formation and evolution of voids in Cu structures.

Parameters that influence electromigration are temperature and current density. Therefore, electromigration becomes increasingly significant as interconnect dimensions shrink since the current densities in the metal lines continue to increase, which results in a degradation of electromigration lifetime. In addition, copper microstructure, interfaces and impurities have to be considered since these parameters influence the effective Cu diffusivities.

Electromigration is not new to science. First observations were reported in molten alloys of lead-tin and mercury-sodium by Geradin in 1861 [4]. Skaupy originated the use of the term “electron wind” in 1914 [5]. Systematic studies of electromigration started in the 1950s by Seith and Wever [6]. They found that the effect of electromigration can be reversed and that the direction is dependent on the majority charge carriers, i.e. electrons or holes. They also established a method to measure electromigration by observing the displacement of an indentation in a metal which is called “marker motion” technique or vacancy flux method [4]. Independently, Fiks in 1959 [7] and Huntington and Grone in 1961 [8] treated the “electron wind” driving force with a semiclassical “ballistic” approach theoretically. When the impact of electromigration became known to the semiconductor industry, numerous studies and publications followed [9]. Up to today, electromigration has remained a major reliability concern.

The relentless miniaturization and downscaling of microprocessors and other semiconductor units leads to smaller and smaller cross-sections of interconnects and the current density keeps increasing. Fig. 1.1 shows the development of the maximum current density j_{max} for the recent past and for the following years. The current density j_{max} will reach 3 MA/cm^2 at 105°C by 2015. With increasing current density, the electromigration-induced damage will increase, which will cause a big challenge for reliability engineers. Further, the advent of new materials in back end-of-line (BEOL) processes (interconnect metallization) complicates the guarantee of reliability. Interconnects used to be surrounded by rigid SiO_2. To reduce resistance-capacitance delay and increase chip signal propagation speed, materials with a low dielectric constant (low k) were introduced. These are usually dense or porous organosilicate glasses (OSG) or other organic materials with inferior mechanical and thermal properties. A number of problems are generated by the introduction of low k materials such as thermally or mechanically induced cracking or delamination [10] and etch damage [11]. Very special care must be provided in today's copper low k interconnect technology to produce chips with the necessary reliability.

1.1 Interconnect Fabrication

Cu was introduced as metallization material by IBM in 1998 [3, 12]. The deposition process changed with the switch from Al to Cu interconnect technology. Al used to be deposited as a whole metal film onto an underlying

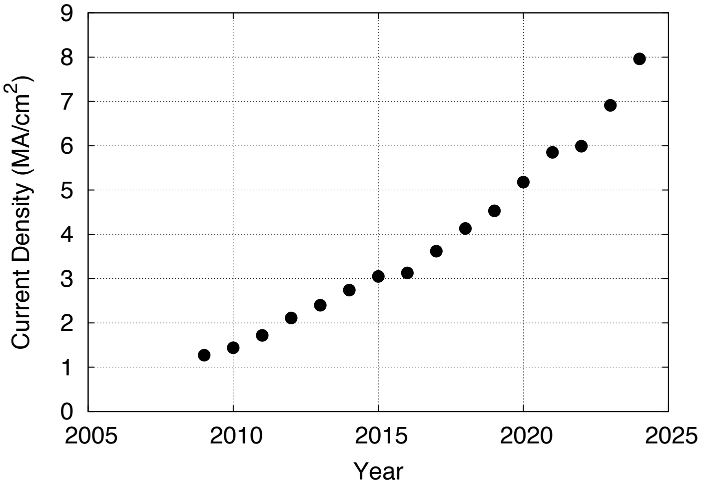


Figure 1.1: Current density j_{max} as function of time according to the ITRS 2010 Update [1].

dielectric, usually SiO_2. After this step, the Al was patterned into interconnects by lithography and etch processes. A similar subtractive etch process does not exist for Cu BEOL manufacturing due to the difficulty of reactive ion etching (RIE) of Cu structures [11, 13]. For Cu technology, a damascene process was developed, where trenches and vias are patterned into the dielectrics using photolithography and RIE. Later, these trenches and vias will form the interconnects. The damascene process enables the extension to deep sub-micron line dimensions with high aspect ratios. The trench side walls, bottoms and the remaining dielectric film are covered with a thin liner material (Ta, TaN or Ta-based compound) using physical vapor deposition (PVD). This liner material serves as a diffusion barrier to avoid corrosion and electric leakage between adjacent metal lines [14]. Subsequently, a copper seed layer is deposited by PVD. A bath in a Cu solution follows where with an applied voltage the trenches and vias are filled with Cu, a process called electroplating. This task is continued until an overburden layer of Cu exists above the trenches and the rest of the dielectric layer. After annealing and stabilizing of the copper structure at low temperature (150-250°C), the overburden is polished away using a chemical-mechanical polish (CMP) step to isolate the Cu structures. Finally, a capping layer (SiN or SiCN) is deposited. The process cycle from trench and via patterning to Cu seed deposition, electroplating, CMP, and deposition of a capping layer is repeated until the full interconnect layer stack is completed.

There are basically two damascene processes: the single and the dual damascene process scheme. For the single damascene process, trench and via are patterned in two separate steps. In contrast, trenches and vias are patterned simultaneously in the dual damascene process. For most of the advanced interconnect circuits the dual damascene process is used. Only one metal filling step is required for the dual damascene process, which results in lower via resistivity and and can result in improved electromigration reliability compared to the single damascene process. The disadvantage of the dual damascene process is the high aspect ratio that results from patterning trench and via simultaneously. This high aspect ratio makes etching, cleaning and Cu filling more complicated, and gives rise to more challenges for integration, causing further reliability issues.

1.2 Motivation

Besides theoretical work, extensive electromigration tests have been performed in the semiconductor industry over the past decades. Since the required lifetime for interconnect systems is in the range of 10 years [15], electromigration testing must be carried out under accelerated conditions. Therefore, the electromigration test temperature is set to 200 to 350 °C and the testing current density is set to several MA/cm^2. Models like the one of J.R. Black [16] are used to extrapolate the electromigration lifetimes to use conditions (≈105 °C and a maximum current density as shown in Fig. 1.1). The lifetimes of identical interconnects under the same test conditions typically follow a log-normal distribution, meaning that the logarithms of the lifetimes follow a Gaussian curve. A large number of interconnects must be tested in order to make the experiment accurately determine the lifetimes for low failure probabilities. For example, a microprocessor has billions of interconnects and even one fail can be critical. Numerable parameters like temperature, fabrication conditions, current density, interconnect geometry etc. must be considered. This is the reason why a third approach, besides theory and physical testing, is desired to assist the experiment, to deepen the understanding of the physics of electromigration and to reveal new insights: computer simulation.

In a computer simulation, costs and efforts are relatively low compared to physical testing, and it is easier to control parameters that affect the results. Undesired variations of for instance process parameters can be excluded, and a decoupling of conditions that influence the results can be more easily achieved. This big advantage of computer simulation for the understanding of electromigration will be demonstrated in the dissertation. A second motivation of computer simulation is to prove the theory and to validate the model that went into the simulation. It is a big success when physical observations can be reproduced via a computer simulation.

The material of metallization for on-chip interconnects is polycrystalline copper with a particular microstructure. That means copper grains are tightly packed together, forming the interconnect. The electrotransport, or electromigration, of copper takes place predominantly along fast diffusion pathways. This is usually the top interface mainly because of the plasma-enhanced chemical vapor deposition (PE-CVD) process, which introduces a lot of energy into the top layer of Cu [17]. The microstructure of interconnects can basically occur in two varieties: polycrystalline and bamboo. If the average grain diameter is much smaller than the interconnect line width or height, the line has a so-called polycrystalline structure. In the other case, if the grain diameter is in the range of the interconnect width or height, the line has a so-called bamboo structure. The bamboo structure is usually desired, because it shows no grain boundaries in the current direction for interconnect lines. Grain boundaries are also fast diffusion paths, but if they do not have components in the current direction, the transport of copper along grain boundaries in bamboo lines can be neglected. Hu et al. [18] showed that small grains appear mainly at the bottom of the interconnect when the line width becomes narrower than 100 nm. A bamboo structure can not be obtained, and the transport of material along grain boundaries can not be neglected anymore. Though it is known that the transport along grain boundaries is orders of magnitude lower than that along the top interface with conventional SiN_x capping layers, novel capping layers like CoWP greatly limit the transport along the top interface. For such capping layers, the amount of mass transport under EM along grain boundaries can become comparable to that transported along the top interface. As a result, the microstructure can significantly affect electromigration and the failure mechanism [19, 20].

In EM experiments, it is difficult if not entirely impossible to control the grain size and grain distribution in interconnects, especially for sub-100 nm lines. In a computer simulation it is possible, thus the primary motivation of the study in this dissertation is to simulate the effect of microstructure on electromigration. In the following a list of few dissertation statements will be presented that will be reviewed in the discussion chapter of this dissertation. The items are claims which this dissertation sets out to accomplish. The claims are listed here in the beginning and discussed in the end, and such set the frame of the dissertation.

1. The computer program developed in this work simulates electromigration reasonably well for a two-dimensional interconnect segment.
2. The model for electromigration simulation developed in this work can predict where material will be depleted, i.e. where voids nucleate in an interconnect segment.
3. The program simulates the growth of voids reasonably well.
4. The simulated electromigration lifetimes follow a log-normal distribution
5. The simulation reflects qualitatively the trend of the effect of small and large grains, as well as strong and weak top interfaces, which is consistent with physical experiments.
6. The software can be used for quantitative analysis.

The primary goal is the simulation of electromigration for two-dimensional interconnect segments, as in item 1. To model the resistance change that leads to failure, void nucleation and growth must be implemented, which is stated by item 2 and 3. As a justification of the model, the failure times must follow a log-normal distribution as observed in physical experiments (item 4). In addition to simulating electromigration in general, the most important implementation is the effect of microstructure. Observations from physical experiments exist that show the dependence of electromigration lifetimes for small and large grain structures. Since the dissertation sets out to model the effects of microstructure, it is pertinent to support the observations from physical experiment with the results from the simulation, as in item 5. The last item 6 (quantitative analysis) was an initial goal of the dissertation, which turned out to be not possible in the scope of the dissertation due to the complexity of the task. To anticipate the conclusion of the discussion chapter, the last item will be answered negatively.

1.3 Scope of this Work

In chapter 2 methods, techniques and setup of the simulations approaches applied in this dissertation will be presented. The log-normal distribution will be discussed as well as the parallel computer Lonestar, on which the simulations were run.

Chapter 3 will deal with the generation of microstructure for the two-dimensional interconnect segments later used in chapter 4. The Monte Carlo technique for grain growth, the Potts Model, will be introduced.

In chapter 4 the phenomenon of electromigration will be reviewed. Subsequently, the model for the electromigration simulation of this work will be introduced. Furthermore, the algorithm for the electromigration simulation on a two-dimensional interconnect segment will be described. The description includes the algorithm for the void growth.

Chapter 5 is about the statistical analysis of the simulated electromigration lifetimes. A failure criterion of electrical resistance increase for two-dimensional interconnect segments will be introduced. Several results will be presented, including the study about small/large grains and weak/strong top interfaces. A comparison with experiments is part of the presentation.

Chapter 6 will discuss the results and will review the dissertation statements of this introductory chapter.

In chapter 7 a summary will be given and possible future work will be outlined.

Chapter 2

Statistical Methods and Simulation Techniques

2.1 The Log-normal Distribution

It is empirically well established that electromigration lifetimes of on-chip interconnects follow a log-normal distribution [21, 22]. The reason why this is so is not well understood so far. One explanation is the log-normal distribution behavior of the microstructure grains of the tested interconnects. In a log-normal distribution the logarithms of the values (e.g. lifetimes or grain sizes) are normally distributed. In the following, the log-normal distribution is discussed with regard to electromigration lifetimes. An example of a log-normal grain size distribution will be given later in this section.

The median time-to-failure is defined as the average of the logarithmic times-to-failure:

$$ln(\bar{t}_F) = \frac{1}{N}\sum_{i=1}^{N} ln(t_{F,i}), \tag{2.1}$$

where N is the number of tested structures. The standard deviation is given by

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(ln(t_{F,i}) - ln(\bar{t}_F))^2}. \tag{2.2}$$

In a log-normal plot, the rank h_i is plotted in a probability scale in dependence on time, which is plotted in a logarithmic scale. The rank is also called the cumulative failure frequency of the i-th structure and is calculated as

$$h_i = \frac{i - 0.3}{N + 0.4} \tag{2.3}$$

after the N failure times have been sorted with increasing time.

2.1.1 Example EM failure times

Suppose a computational failure experiment yielded the data presented in Table 2.1. The median time-to-fail is 213.55 and the standard deviation σ is 0.41, according to Table 2.2. The distribution h_i over time-to-fail is shown in Figure 2.1. In this probability scale vs. logarithmic scale, the date points ($\bar{t}_{F,i}$,h_i) can be approximated by a line, which means that these data points follow a log-normal distribution. Given median and sigma, a line can be drawn through the data points as a fit by integrating the probability density function

$$PDF(t) = \frac{1}{\sqrt{2\pi}\sigma t} exp\left(-\frac{(ln(t) - ln(\bar{t}_F))^2}{2\sigma^2}\right) \tag{2.4}$$

such that one obtains the cumulative distribution function

$$CDF(t) = \int_{-\infty}^{t} PDF(\tau)\,\mathrm{d}\tau = \frac{1}{2}\left[1 + erf\left(\frac{ln(t) - ln(\bar{t}_F)}{\sigma\sqrt{2}}\right)\right], \tag{2.5}$$

where erf is the error function.

2.1.2 Example Grain Size Data

A two-dimensional Monte Carlo Potts model simulation yielded the microstructure of Figure 2.2a (for a detailed description of grain growth mod-

i	$t_{F,i}$ in a. u.	rank h_i	h_i in %
1	125	0.07	7
2	147	0.16	16
3	162	0.26	26
4	174	0.36	36
5	195	0.45	45
6	213	0.55	55
7	238	0.67	67
8	257	0.74	74
9	276	0.84	84
10	543	0.93	93

Table 2.1: Example EM failure data to show log-normal failure times and corresponding h_i as plotted in Figure 2.1. N=10.

N	$ln(\bar{t}_F)$	$\bar{t}_F$	σ
10	5.36	213.55	0.41

Table 2.2: Statistics for the example data presented in Table 2.1

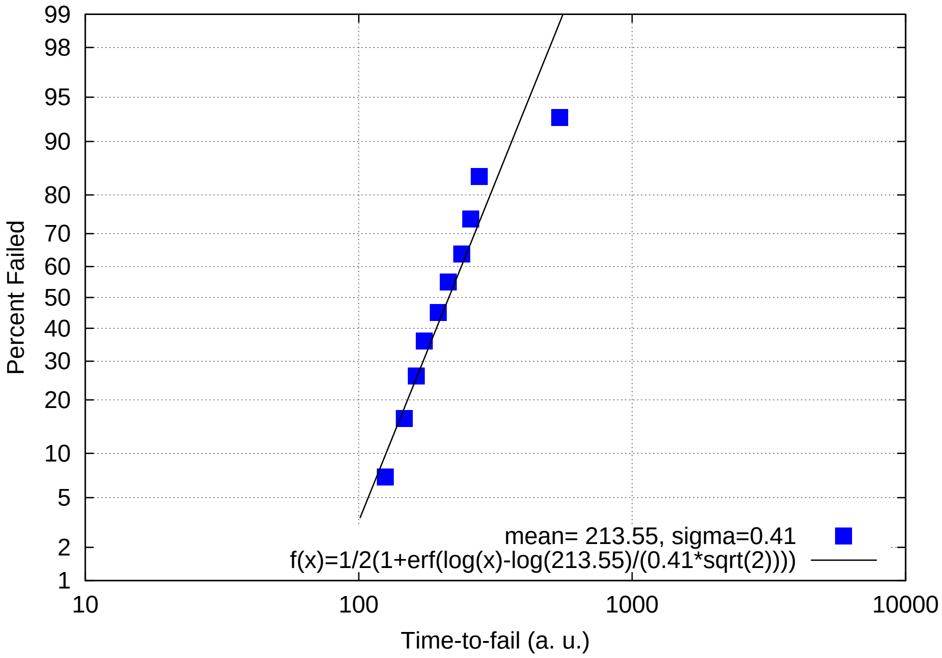


Figure 2.1: Log-normal plot of the example EM failure data from Table 2.1 with $ln(\bar{t}_F)$=5.36, $\bar{t}_F$=213.55 and σ=0.41

eling see Section 3.1). The width and the height were set to 300 and 100 units, respectively. As can be seen in the picture, only 7 grains are left inside the computation domain. The sizes of these grains are listed in Table 2.3. Here, the size refers to the diameter and is calculated as the square root of the grain area in square units. The log-normal grain size distribution is characterized by a median grain size of 50.40 and a sigma of 0.62, as shown in Table 2.4. The data is plotted in Figure 2.2b.

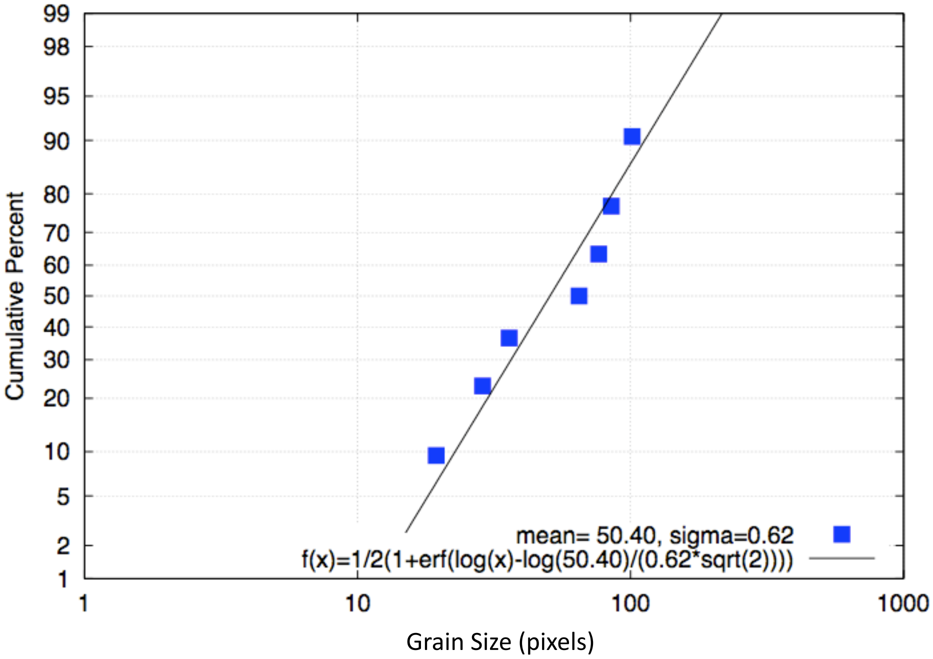
i	grain diameter in units (pixels)	rank h_i	h_i in %
1	19.4	0.09	9
2	28.7	0.23	23
3	35.9	0.36	36
4	64.7	0.50	50
5	76.5	0.64	64
6	84.1	0.77	77
7	101.3	0.91	91

Table 2.3: Example data to show grain sizes and corresponding h_i as plotted in Figure 2.2. N=10.

N	$ln(\bar{d})$	$\bar{d}$	σ
7	3.92	50.40	0.62

Table 2.4: Grain size statistics for the example data presented in Table 2.1

(a)

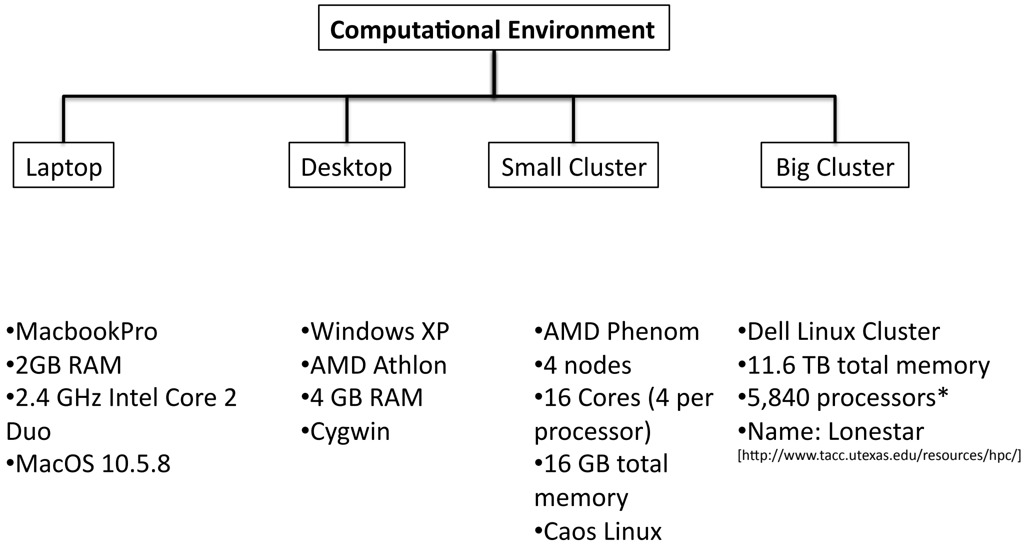


(b)

Figure 2.2: (a) Image of the microstructure (b) Log-normal plot of the example data from Table 2.3 with $ln(\bar{d})$=3.92, $\bar{d}$=50.40 and σ=0.62

2.2 Computational setup

Figure 2.3 shows an overview of the computing hardware used for the simulations in this dissertation. Basically, a laptop (MacBook Pro) and a desktop computer (AMD Athlon) were used for the development of the simulation code. The programming language was C/C++. A small linux cluster consisting of 4 nodes with 4 cores each was employed for simulation testing in a parallel environment. Overall, the statistics on the small linux cluster were not enough. Only 16 electromigration simulations could be run on it simultaneously. A population of 100 interconnect segments for a single electromigration simulation test was desired. These computations were carried out on the big linux cluster, the Dell Linux Cluster Lonestar at the Texas



*only 100 processors were used per electromigration simulation

Figure 2.3: Organizational chart illustrating the computing environment

Advanced Computing Center at the University of Texas at Austin.

2.2.1 The Small Linux cluster

The cluster consists of 4 nodes and every node consists of 4 cores. Thus, the cluster is composed of 16 parts, where the number of parts is the product of nodes and cores. AMD Phenom processors were used for the cluster. 4 GB of RAM were built into every node.

For the grain growth, each cell or volume element uses one byte. Considering an operating system overhead of 500 MB, 3.5 GB are left for the grain growth. With this amount of memory geometries with 3.5 billion cells are possible to compute. Therefore, lattices of 1000x1000x1000 cells can be modeled. With 4 nodes and 4 GB RAM each, leaving 500 MB for the operating system, an overall of 14 billion cells can be computed by the cluster in the grain growth simulations.

For the void growth and electromigration modeling the memory requirement is much higher and set at 48 bytes per cell. Using 3.5 GB of free RAM, geometries with 78 million cells per node are feasible. With a cross-section of 1000x1000 cells, 78 slices can be computed per node. This corresponds to 312 slices for all 4 nodes. The maximum resolution is therefore 1000x1000x312 cells.

The nodes are subdivided into one head node and 3 working nodes. For distributed computing, the head node is also engaged. It is easily possible to extend the cluster by further nodes. The IP addresses are assigned automatically and the working nodes are booted through the network, i.e. no operating system needs to be installed on the working nodes. Just the network boot option must be activated in the BIOS. The file systems of the working nodes are integrated into the file system of the head node.

The Caos Linux operating system was chosen. Multiple Linux distributions were tested, among them Rocks, CentOS 5 and Fedora 10. Only one distribution complied with the hardware, which was Caos Linux. Additionally, Caos Linux includes all the necessary cluster software and installation of further cluster software is not necessary.

The nodes are connected through Gigabit ethernet and a switch. A disadvantage of the setup, as it turned out, is that the nodes need to be restarted regularly.

Access to the cluster is provided via ssh-terminal.

The nodes were provided with mains adapters that were designed for 24 h operation.

Table 2.5 lists the runtimes of the cluster for the grain growth simulation. A lattice of 1000x200x200 cells (40 million cells) was modeled for the computations. The calculation ran for 10 Monte Carlo time steps (MCS). One MCS means that every cell was given the chance to switch its orientation.

The runtimes in table 2.5 scale almost linearly, except for the 1x1 and 2x1 case where the computation times are comparable. For the 2x2 and 1x4 case an acceleration by the factor two can be observed. Theoretically, an acceleration by the factor 8 can be expected when calculating with 16 parts.

2.2.2 The Dell Linux Cluster Lonestar

In order to gather sufficient statistics for an electromigration simulation run, the Dell Linux Cluster Lonestar at the Texas Advanced Computing Center (TACC) at the University of Texas at Austin was employed. The machine was comprised of 5,840 processors and was composed of 11.6 TB total memory, although only 100 processors were used for a single electromigration simulation for a population of 100 interconnect segments containing different microstructures.

Nodes x Cores	Parts	Runtime
1x1	1 parts	3m59.157s
1x4	4 parts	2m05.712s
2x1	2 parts	3m57.462s
2x2	4 parts	2m06.566s
2x4	8 parts	1m12.106s

Table 2.5: Runtimes for parallel computation of grain growth on the small cluster.

Chapter 3

Simulation of Grain Growth

The goal is to conduct statistical simulations to obtain electromigration lifetime distributions with dependence on microstructure. Hence it is necessary to generate a pool of different microstructures as input for the electromigration simulation. The technique used for the microstructure generation will be discussed in this chapter.

3.1 Monte Carlo Grain Growth - The Potts Model

A Monte Carlo method based on the modified Potts model was used to simulate the grain growth. The Potts model [23] is a generalization of the Ising model [24]. In the Ising model, a site in a lattice can take one of two magnetic spin states (spin up or spin down). Domains of the same spin can grow by minimizing the boundary between the domains. The Potts model is an extension of the Ising model in the sense that an arbitrary number of spin states is possible. In the early 1980s, long after the Ising (1925) [24] and Potts (1952) [23] models were devised, the similarity between the magnetic spin state domains of the Potts model and grain structures of polycrystals was recognized, and the Potts model was proposed for grain growth simulation applications [25, 26, 27].

What follows is a description of the modified Potts model. Further details can be found in a number of references [25, 28, 29, 30, 31, 32, 33, 34, 35].

In the beginning of the simulation, a lattice is filled with random integers, ranging from 1 to Q, where Q was fixed at 30. Q is the number of spin states in the Potts model. For the grain growth, Q is the number of different crystallographic orientations (qualitatively). The number 30, a large number for the Potts model, was chosen to prevent frequent impinging of grains with the same orientation during grain growth. The lattice was chosen to be orthogonal. Usually, a trigonal lattice is used for the two-dimensional case. Since the algorithm was developed for three dimensions, where an orthogonal lattice is more practical, the orthogonal lattice was used for two dimensions as well for convenience, applying the same computer program. Only two-dimensional microstructures were generated for the electromigration simulation.

After allocating the random indices onto the lattice, reorientation attempts are undertaken. For this, a site is randomly selected. The number of unlike neighbors (neighbors with a different orientation) is counted, which corresponds to the energy of the site. Here, the neighbors are the left, right, top, bottom and the four diagonal sites. The energy Hamiltonian for the site i can be written as [34]

$$E = J_i \sum_{j}^{n} (1 - \delta_{S_i S_j}) + H_i, \tag{3.1}$$

where $\delta_{S_i S_j}$ is the Kronecker delta and S_i and S_j are the orientation indices of site i and j respectively. J_i is the grain boundary energy which is set to

1 in this simulation, regardless of the orientation index. H_i is the volume or surface energy, depending on the location of the site i. For a constant volume energy H_i and an isotropic grain boundary $J_i = J$, the grain growth is expected to be normal and isotropic [32]. In this simulation the volume energy was set to 0 uniformly, not taking into account surface or interface effects. This circumstance means that the Potts model, which is employed here, only simulates curvature-driven growth. Due to the lack of any volume or surface energy there is no other driving force that could cause the grain boundaries to migrate. Implementing the surface or volume energy can be done in future work.

The orientation of the site i is set to one of the unlike neighbors, chosen at random with equal probability, and the energy is recalculated. If the energy has decreased compared to the state before the reorientation, then the new orientation is kept. If the energy is larger or equal, then the new orientation is kept with the Boltzmann probability

$$p = exp\left(\frac{-Q}{k_B T}\right), \tag{3.2}$$

where Q is the activation energy for grain boundary migration, k_B is the Boltzmann constant and T is the simulation temperature. Since Q cannot be determined explicitly and the energy of the Hamiltonian (Equation 3.1) is on an arbitrary scale, Equation 3.2 is simplified to [34]

$$p = exp(-2\Delta E), \tag{3.3}$$

where ΔE is the energy difference before and after the reorientation. Subsequently, a new site is chosen at random. Particularly, it is chosen from the rest of the lattice sites, excluding the one that has already been subjected to a reorientation attempt. In this way, the sites are traversed in order of a permutation. When no site is left, the simulation time is increased by one Monte Carlo step (MCS). This is a modified version of the Monte Carlo technique used for grain growth, since the sites are traversed in a permutation and not in a purely random manner (where the already subjected sites are not excluded from further reorientation attempts). The decision to use this method was made to increase the efficiency of the algorithm. With the permutation, exactly every site is given the chance to reorient. After N such reorientation attempts (where N is the number of lattice sites), the attempts restart with a new permutation.

3.2 Grain growth simulation results

Typical results for the simulation of grain growth are shown in Figures 3.1 to 3.5. These figures depict a segment of a Cu interconnect segment. Figure 3.1a-g shows the evolution of grain growth in two dimensions. The Monte Carlo time step numbers for this Figure are 0, 100, 200, 300, 800, 1600 and 3200. The resolution is set to 300x100 volume elements. For calculations in two dimensions the same algorithm is applied as for the three dimensional case. For the two dimensional case the width is set to 1 volume element. Therefore, the resolution is 300x1x100 in XxYxZ. Here, X corresponds to the length, Y to the depth and Z to the height of the Cu interconnect segment shown in Figure 3.1. The random seed that was used to initialize the distribution of crystallographic orientations was set to 3000.

A modified Potts model was used for the Monte Carlo calculations. The Potts model is well suited for the simulation of grain growth of polycrystalline materials, as described in the previous Section 3.1. In Figure 3.1b-g the typical angle of 120 degrees between grain boundaries can be observed. The transition from a polycrystalline structure in Figure 3.1b-e to a bamboo structure in Figure 3.1e-f can be seen.

Some of the grains in Figure 3.1 appear non-physical, for instance the left grain in Figure 3.1f, which has a concave shape. The concave boundaries are caused by the following circumstance. At the junctions of the grain boundaries with the boundaries of the computational domain, the grain boundaries are all nearly perpendicular. The perpendicularity is caused by the curvature-driven grain growth. At the junction, the curvature becomes zero, and growth is minimized, pinning the grain boundary at 90°. When the grain boundary is pinned at 90°, and the intersection at the other end of the grain boundary is pinned at 120° for a grain boundary triple point, there must be a concave transition at least for one bordering grain between the two angles. If there was surface energy incorporated, cute angles between the grain boundaries and the boundary of the computational domain are possible, minimizing the need for a concave transition. The implementation of surface energy can be done in future work. The non-phyiscal concave grain shape is tolerated in the present calculations.

Figure 3.2 shows the relationship between the mean grain radius R and the Monte Carlo time steps. In the two dimensional case, the grain radius is calculated as the square root of the number of volume elements the grain consists of. The progression of the mean grain radius in dependence on Monte Carlo steps resembles closely a square root function. The steps in the curve are characteristic for the limited extent of the interconnect segment. For the first 100 time steps in Figure 3.2b the steps in the curve are not very pronounced yet. More precisely, the steps are branches that decrease. Disappearing grains are the cause of this behavior. Grains generally grow at the expense of other shrinking grains. The grain radius of a shrinking grain eventually becomes so small that it has an influence on the mean grain radius. Thus, the mean grain radius is decreasing despite of the continuation of the grain growth algorithm. This can explain the decreasing branches of the mean grain radius curve in Figure 3.2. When the shrinking grain finally disappears, the mean grain radius increases in a step-like fashion. The absence of the disappeared grain is a discontinuous event which is the cause for the jump in the mean grain radius curve. If one chooses an interconnect segment with a sufficient extent such that the grain sizes are much smaller than the length and height of the segment, the steps in the curve will be less pronounced, approaching a root function.

Figure 3.2 is only one example for the evolution of grain size in dependence on MCS for one configuration. For different configurations, the curve deviates substantially from the one shown. Figure 3.3a shows the spread of the curves for 100 configurations. In Figure 3.3b, the mean grain size was averaged over the 100 configuration for each MCS and the result is displayed in a single curve with the standard deviation (sigma) as error bars. It can be seen that the standard deviation increases for evolving MCS. This behavior makes it impossible for the grain growth algorithm to generate a microstructure with a specified sigma in grain size. This could be important when trying to compare the grain distribution sigma with the electromigration lifetime distribution sigma, which is later discussed in Chapter 4. The modified Potts model that was used is not suited for generating microstructures with a specified sigma and only specified grain sizes can be obtained. Studies of the effect of electromigration lifetime distribution sigma on grain size distribution sigma can not be conducted. The modified Potts model is limited to producing microstructures of specified grain size.

From Figure 3.3b, the grain growth exponent can be extracted. The evolution of the mean grain size can be fitted with a function with the from of $\bar{R}$=c*t^n, where $\bar{R}$ is the mean grain size, c is a constant, t is the time in MCS and n is the grain growth exponent. From the least squares fit in Figure 3.3b, the grain growth exponent is derived to be 0.49. This is in excellent agreement with other works in the literature. For example, Anderson and Grest [28] have reported a power law kinetics for grain growth with a growth exponent of 0.48±0.04.

In the literature it is said that the number of different grain orientations Q in the Potts model has an influence on the grain growth exponent. For instance, Chen and Yang [36] found that n decreases linearly for $2 \leq Q \leq 30$ and is close to a constant of 0.41 for $Q \geq 30$. However, they also state that for large systems and very long simulation runtimes the grain growth exponent is 0.5. To verify this, a simulation experiment has been conducted to study the influence of Q on the grain growth exponent. The result is shown in Figure 3.4. Q was varied between 5 and 75 with a step width of 5. For each Q, 5 configurations were evaluated and averaged. What can be seen in this Figure is that there is no significant dependence on Q for the grain growth exponent. The overall growth exponent was found to be 0.48 for all Q. This is close to the value of 0.5, however large systems and very long runtimes were not used. The system was 300×100 units^2 in size and the runtime was 1000 MCS.

Figure 3.5a-d shows the three dimensional grain growth simulation in an interconnect piece that has a resolution of 300x100x100 units^3.

The algorithm for the grain growth simulation was made to run in parallel on the cluster.

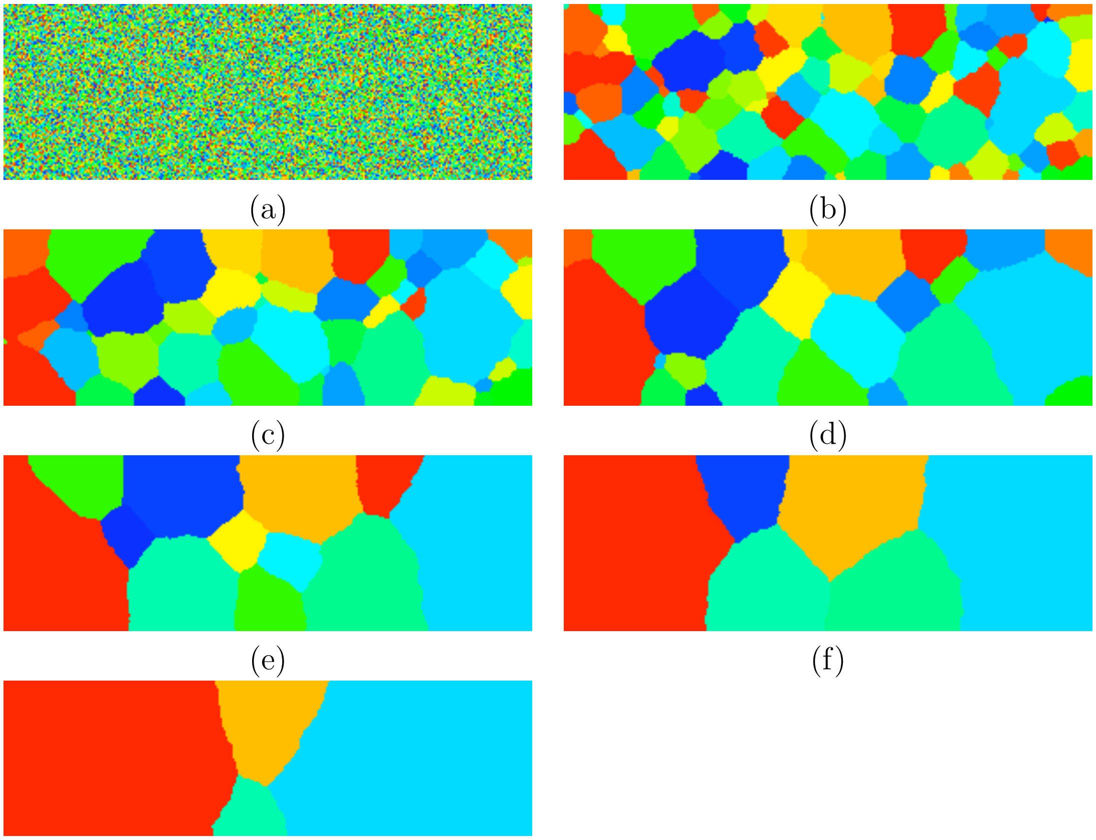
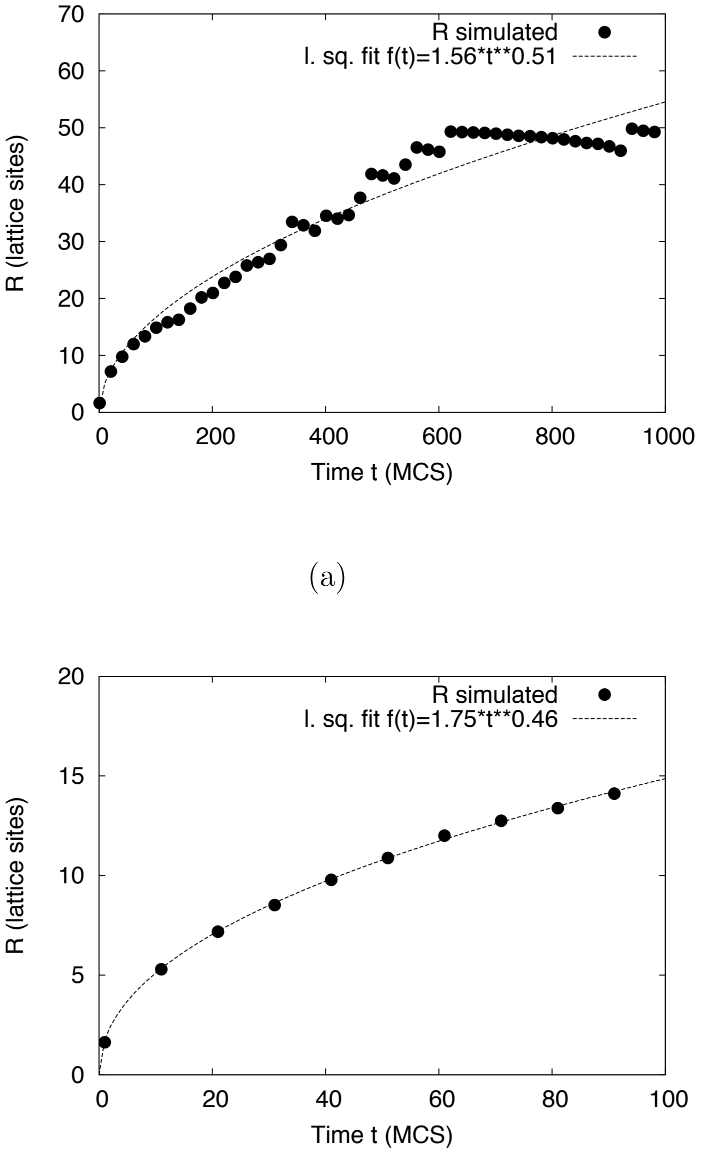

(a) (b) (c) (d) (e) (f) (g)

Figure 3.1: Evolution of microstructure using the modified Potts model. (a) 0 Monte Carlo steps, (b) 100, (c) 200, (d) 400, (e) 800, (f) 1600 and (g) 3200.



(a)

(b)

Figure 3.2: (a) Evolution of the mean grain size R in dependence on the Monte Carlo steps for the interconnect segment in Figure 3.1. (b) Magnified view of (a) for the first 100 Monte Carlo steps.

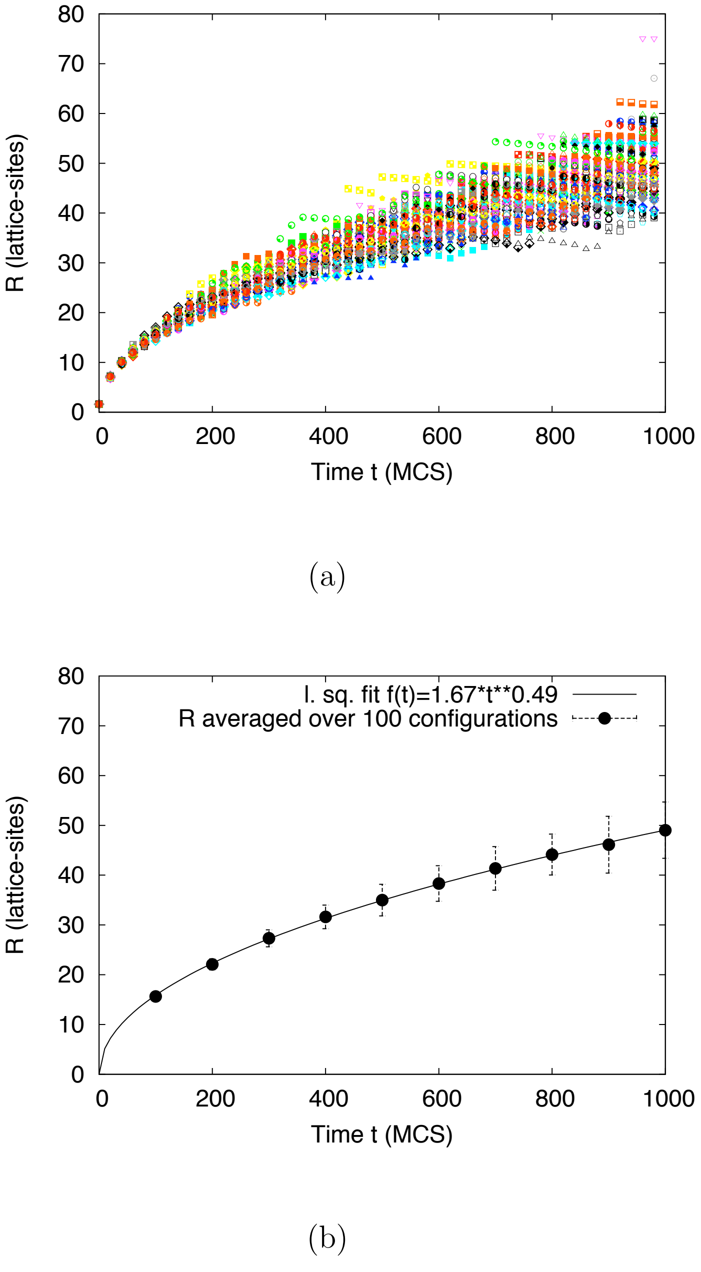


Figure 3.3: (a) Evolution of the mean grain size R in dependence on the Monte Carlo steps for 100 configurations showing the spread in grain size. (b) Averaged grain sizes of (a) with the standard deviation as error bars.

MCS	$\bar{R}$ (lattice sites)	sigma
100	16	0.60
200	22	1.12
300	27	1.71
400	32	2.37
500	35	3.17
600	38	3.57
700	41	4.37
800	44	4.10
900	46	5.70
1000	49	5.66
2000	69[1]	

Table 3.1: List of mean grain size $\bar{R}$ as function of MCS as shown in Figure 3.3. The values are averaged over 100 configurations.

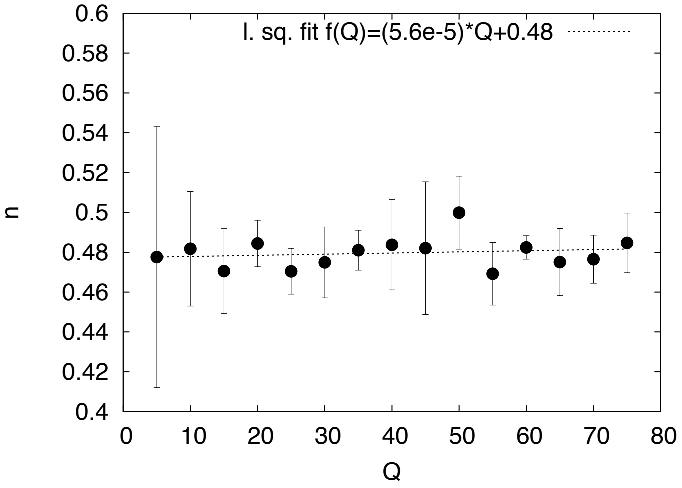
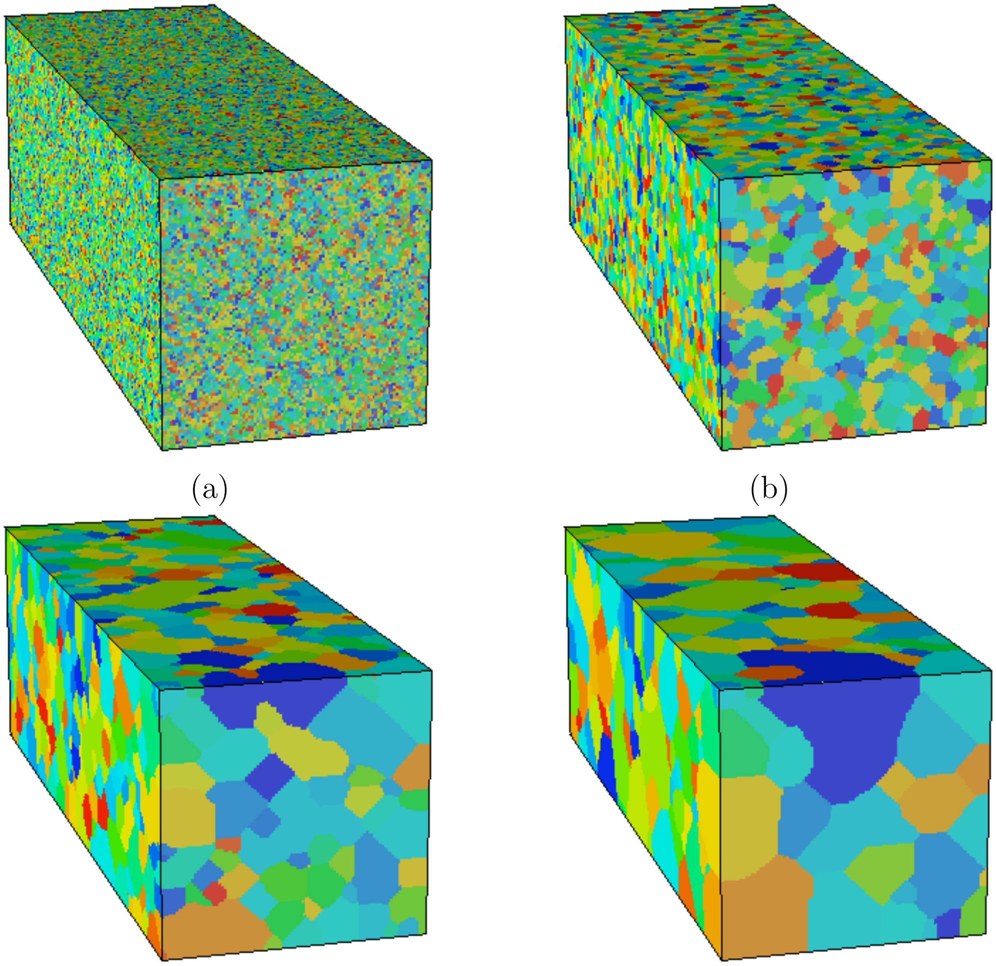


Figure 3.4: Domain growth exponent n as function of Q. The values for each Q have been averaged over 5 configurations. The exponent n shows no statistically significant dependence of Q. The overall growth exponent is ≈ 0.48.



(a) (b)

(c) (d)

Figure 3.5: 3D Evolution of microstructure using the modified Potts model. (a) 0, (b) 10 ,(c) 100 and (d) 250 Monte Carlo steps.

Chapter 4

Electromigration

Electromigration is the movement of atoms caused by an applied electric field and current. Through momentum transfer from electrons to the atoms, the atoms move from their equilibrium position and can eventually jump into a neighboring free lattice site. The atoms migrate in the direction of electron flow. For a basic understanding of electromigration, the terms electron wind and electron wind force are often used in the literature.

The discovery of electromigration can be traced back to 1861, when Gerardin first observed the phenomenon in molten lead-tin and mercury-sodium alloys [4]. But it was not before the the 1950s, when systematic research of electromigration began. One of the first studies can be found in Ref. [6]. Intense investigation of the electromigration phenomenon started in 1966, when all major semiconductor companies (Fairchild, Texas Instruments, Motorola and IBM) reported a new failure mechanism due to electromigration in aluminum interconnects of integrated circuits [37, 22]. For a short period of time, the existence of integrated circuit industry was threatened [15].

Besides interconnects, which are the wiring between devices on a computer chip, the electromigration phenomenon can also be observed in solder joints. In the following, only electromigration in on-chip interconnects will be regarded.

Interconnects on a chip are arranged in patterned layers, and the vertical connects are referred to as contacts or vias. From the 1960s to the 1990s, interconnects were fabricated with aluminum, and from the late 1990s, after the introduction of a commercial copper process by IBM, the industry started to shift to copper as the conductive material. Copper has a lower resistivity than aluminum, which allows faster signal propagation in the product.

Electromigration in Cu interconnects causes a mass transport, i.e., movement of Cu atoms, from the cathode end to the anode side. This means, upstream depletion and voiding can be observed and sometimes downstream accumulation and hillocking. Consequently, two major failure modes can occur: Firstly, owing to the voiding process, the electrical resistance can rise above the operational limit. Secondly, the hillocking can cause an electrical short with an adjacent interconnect.

Electromigration is a process that can take months or years in a chip operated under use conditions to show an effect. Nevertheless, electromigration has been a major reliability concern for the past forty years when taking into account that the warranty of a chip should be at least 7 years for the consumer market and 10 years for commercial applications. Thus, elaborate electromigration testing is necessary to ensure reliability. Since it is not practicable to test interconnects under use conditions for months and years, they are tested under accelerated conditions, which means typically temperatures in a range from 250 to 350°C and one to several MA/cm^2.

The time to fail is called the lifetime of the interconnect. When testing a population of equal interconnects, the lifetimes typically follow a log-normal distribution, which means that the logarithms of the lifetimes are normally distributed. Two parameters of the lifetime distribution are of importance: the mean time to fail t_{50} and the standard deviation sigma. In a log-normal plot, i.e., the y-axis as a probability scale and the x-axis as a logarithmic time scale, log-normally distributed lifetimes follow a straight line, with the sigma reflecting the slope where a big slope corresponds to a small sigma. Generally, for better electromigration behavior, i.e., less electromigration damage, t_{50} should be high. At the same time, sigma must be small, because a high mean time to fail can be counteracted by a large sigma. That is because even a single failed interconnect can lead to the failure of a chip. Therefore it is important that all fail times remain tightly around t_{50}. If this is not the case, an interconnect might fail very early.

The distribution can be multimodal, which means that some data points are far from the fitting line and can be fitted by an additional line or lines. A bimodal distribution is typical for an early fail mode. In this case, some of the interconnects fail much earlier than the rest. This behavior is typical for a downstream test configuration. In this case, the current flows from a wide metal in an upper metallization level through a via down into a lower metallization layer. The upper metal line is wider because the lower should degrade faster, which is the one to be tested. At the bottom of the via, a diffusion barrier is located, which is inherent from the interconnect fabrication. The barrier prohibits the movement of Cu atoms from the via into the lower metal line. That means, voiding can occur underneath the barrier, which is the cathode end of the lower metal line. Most commonly, when voiding occurs, Cu is depleted through the whole cross-section of the interconnect. In a few cases, a shallow void appears underneath the via. A shallow void takes much less time to grow, but it causes an open circuit. These few cases are called early fails, and the overall lifetimes lead to a bimodal distribution. It is crucial to examine the early fails since they tremendously decrease the lifetime of a chip. In most cases it is not enough to test a population of single interconnects since the experiment is not sensitive enough to early fails - among the limited number of interconnects in the experiment early fails might not occur, unlike on a chip with hundreds of millions of interconnects. In order to catch the early fails, one might chain many interconnects (10, 100, 1000) in a multi-link series. The longer the chain, the more sensitive is the experiment.

A further aspect of electromigration in interconnects is the short length effect, or Blech effect [38, 39, 40]. The depletion of metal atoms upstream and the accumulation downstream, which causes a gradient in Cu concentration, leads to a stress gradient. The stress build-up downstream or at the anode end causes metal atoms to migrate in the opposite direction of the electron flow. This is opposite to the electromigration direction. If the interconnect is short enough and the if stress build-up is high enough, a dynamic equilibrium can be reached where an equal number of atoms move downstream through electromigration as atoms move upstream caused by the stress gradient. In the case of equilibrium, electromigration degradation stops and electromigration will never come to fail the interconnect. Unfortunately, not all interconnects on a chip can be made short enough (shorter than the Blech length).

Cu interconnects are surrounded at the side walls and at the bottom with a liner made of TaN, Ta or a Ta-based compound. The liner provides good adhesion between the Cu and the embedding dielectric, and it serves as a diffusion barrier to prevent diffusion of Cu into the active regions of the chip, i.e., the transistors, as well as to adjacent interconnects, which can create an electric short. The top of the interconnect is covered with a dielectric capping layer made of SiN, SiC or SiCN. Novel approaches add metallic coating, e.g. CoWP, which provides high bonding strength and good adhesion, and it mitigates the electromigration degradation process.

Cu exhibits a microstructure. If the diameter of the copper grains is small compared to the width and height of the interconnect, the microstructure is referred to as polycrystalline. In case that the diameter is similar or larger than the width and height, it is a bamboo structure. The classification is important since the grain boundaries provide fast atom transport pathways for electromigration. A polycrystalline structure has more grain boundaries, hence more fast electromigration pathways, which leads to an accelerated degradation. In contrast, a bamboo structure with nearly vertical grain boundaries does not have as many fast electromigration pathways since the grain boundaries are mostly perpendicular to the electron flow.

Overall, the electromigration pathways are in the order of decreasing migration speed: the top interface (for conventional capping layers), the grain boundaries, the side walls and bottoms, and the Cu bulk. That means, the top interface between Cu and the conventional cappings like SiN_x, SiCN or SiN_xH_y forms the fastest electromigration diffusion path. The reason for this is that the about 2 nm thick intermixing layer between the Cu and the dielectrics at the interface is highly disordered and shows poor adhesion, compared to the liners at the side walls and the bottom. Therefore, voids start to form at the top interface, especially at intersections between grain boundaries and the interface. These intersections are potential sinks for vacancies (lattice sites not occupied by an atom) because they create flux divergent sites, which means that a different amount of material is delivered through electromigration paths leading to the site than is carried away by paths going away from the site. Since the crystallographic orientations of the atoms belonging to the grain boundary are different (otherwise there would not be a grain boundary), electromigration diffusion properties are also different, because these properties depend on the crystallographic orientation. If more material is carried away than delivered, the site is a vacancy sink. A void can nucleate caused by vacancy supersaturation. The void surface is an additional electromigration diffusion path, which is even faster than the top interface. If material is removed from the upstream side of the void and diffuses along the void surface to the downstream side, the void virtually seems to move in the opposite direction, towards the cathode end, where agglomeration of voids leads to the growth of a large void that can fail the interconnect.

4.1 Electromigration models

4.1.1 Black's model

One of the early models to predict median time to failure is the one of J. R. Black (Equation 4.1) [16, 41].

$$t_{50} = Aj^{-n} exp\left(\frac{Q}{kT}\right) \tag{4.1}$$

It is an empirical model, putting in relation a geometrical factor A, the electric current density j, the activation energy Q and the temperature T to calculate the median time to failure (MTF or t_{50}). The current exponent n is set from 1 to 2, depending on the consideration of electron wind force only or joule heating. The model is still widely used today to extrapolate median time to failure from test to use conditions.

4.1.1.1 Extrapolating from test to use conditions

Electromigration tests are usually conducted under accelerated conditions (elevated temperature and current densities). The Black equation helps to extrapolate the median time to failure from these elevated test conditions to use conditions. Equation 4.2 is basically the ratio of two Black equations for both test and use conditions, for which the mean time to fail for use conditions can be extracted.

$$MTF_{use} = MTF_{test}\left(\frac{I_{test}}{I_{use}}\right)^n exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_{test}} - \frac{1}{T_{use}}\right) + N_{stdev}\sigma\right] \tag{4.2}$$

The parameter N specifies the failure percent to which the reliability of the interconnects must be guaranteed for a given use condition, and is determined by product specifications [42]. A higher value of N means a more stringent failure criterion, for example a "6σ" extrapolation (N=6) refers to a cumulative failure percent of 1e-7%, compared to 1e-1% for N=3. The parameter σ is the standard deviation of the logarithms of the failure times, or the inverse slope of log-normal failure distribution, and describes the spread of the failure times.

4.1.2 Kirchheim's model

One of the early models to simulate the effects of electromigration is the one by Kirchheim [43, 44]. It calculates the generation of tensile and compressive stresses by the annihilation and production of vacancies which are subject to driving forces due to electromigration and due to the developing stress gradient. The rate of the stress changes is related to the deviation of the vacancy concentration from its equilibrium concentration. The equilibrium concentration of vacancies in the grain boundaries is

$$c_\sigma = c_0 exp\left(\frac{(1-f)\Omega\sigma}{kT}\right) \tag{4.3}$$

where c_0 is the equilibrium vacancy concentration at zero stress, Ω is the atomic volume, kT has the usual meaning and f ($0 \leq f \leq 1$) denotes the contraction following the relaxation of neighboring atoms at the site of a vacancy. The total flux j can be written as the sum of the Fick diffusion term, the electromigration flux term and the stress gradient flux term as follows:

$$j = -D\frac{\partial c}{\partial x} + \frac{Dc}{kT}Z^* e\rho j_{el} - \frac{Dc}{kT}f\Omega\frac{\partial \sigma}{\partial x} \tag{4.4}$$

where D is the diffusion constant, Z*e is the effective charge, ρ the resistivity and j_{el} is the electric current density. Deriving Fick's second law by using the continuity equation ∂c/∂t=-∂j/∂x, Equation 4.4 becomes

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2} + D\frac{\partial c}{\partial x}\left(-\frac{Z^* e\rho j_{el}}{kT} + \frac{f\Omega}{kT}\frac{\partial\sigma}{\partial x}\right) + \frac{Dc}{kT}f\Omega\frac{\partial^2\sigma}{\partial x^2} - \frac{c-c_0}{\tau_g} \tag{4.5}$$

where a source term $(c-c_0)/\tau_g$ is added describing the annihilation of vacancies if their concentration is larger than the equilibrium value, or the production if their concentration is lower than the equilibrium value.

A relaxed vacancy generates a volume change by ΔV/V=(1-f)Ω and the vacancy generation rate within a grain boundary of thickness δ is given by

$$\frac{1}{V}\frac{\partial V}{\partial t} = (1-f)\Omega\frac{\delta}{d}\frac{\partial c}{\partial t} = (1-f)\Omega\frac{\delta}{d}\frac{c-c_0}{\tau_g} \tag{4.6}$$

where d is the grain diameter. Using Hooke's law $\delta\sigma$=BδV/V, the derivation of the rate of stress change yields

$$\frac{\partial\sigma}{\partial t} = B(1-f)\Omega\frac{\delta}{d}\frac{c-c_0}{\tau_g} \tag{4.7}$$

Using the following dimensionless quantities

$$\xi = \frac{x}{l}, \chi = \frac{c}{c_0}, \theta = \frac{D'}{l^2}, p = \frac{\sigma\Omega}{kT} \tag{4.8}$$

(where l is the length of the grain structure) and choosing characteristic lengths to describe the influence of electromigration and vacancy annihilation or production

$$l_e = \frac{kT}{Z^* e\rho j_{el}}, l_s = \frac{1}{2}\sqrt{D\tau_g} \tag{4.9}$$

Equations 4.5 and 4.7 become the two coupled differential equations that describe the Kirchheim model as follows [44]:

$$\frac{\partial \chi}{\partial \theta} = \frac{\partial^2 \chi}{\partial \xi^2} + \frac{\partial \chi}{\partial \xi}\left(f\frac{\partial p}{\partial \xi} - \frac{l}{l_e}\right) + \chi f\frac{\partial^2 p}{\partial \xi^2} - \left(\frac{l}{2l_s}\right)^2 [\xi - exp((1-f)p)] \quad (4.10)$$

and

$$\frac{\partial p}{\partial \theta} = \frac{(1-f)c_0 B\Omega^2 l^2 \delta}{4kTl_s^2 d}[\chi - exp((1-f)p)]. \quad (4.11)$$

The derivation was done by Kirchheim [44]. Figure 4.1 displays four general cases for the Kirchheim equations. For case I (diffusion dominated) the ratios of l/l$_e$ and l/l$_s$ are set both smaller than 1. For case 2 (vacancy production dominated or source/sink dominated), the ratio l/l$_e$ is smaller than 1 while l/l$_s$ is bigger than 1. For case III (EM dominated), the ratios are the other way around, i.e. l/l$_e$ is bigger than 1 and l/l$_s$ is smaller than one. For the mixed case (source/sink dominated combined with EM dominated) the ratios of l/l$_e$ and l/l$_s$ are both bigger than 1.

Figure 4.2 displays the numerical solutions for the Kirchheim equations for cases I, II and III in one dimension. For case I a steady state is reached with a linear vacancy concentration gradient. For the source/sink dominated case, a steady state is also reached but in a non-linear fashion. The EM dominated case III shows no steady state development. More and more vacancies are transported towards the cathode end (origin of electron flow) with increasing time.

The Kirchheim model is important to the development of the model used in this dissertation, because both models share the same origin. Basically, the model used in this dissertation is the Kirchheim model without the development of stress.

4.1.3 Korhonen's model

A physically based analytical model was proposed by Korhonen [45] to account for the mechanical stress evolution in a confined metal line. The model was originally devised for Al-based interconnects embedded in SiO_2, where grain boundaries provide the fastest diffusion paths for electromigration. The following is a mathematical derivation of the model. The Korhonen model is a very popular model for simulating the evolution of stress in an interconnect line, which is why it is presented here. The Korhonen model was implemented in the MIT/Emsim program, a simulation tool developed at the Massachusetts Institute of Technology in the group of C. V. Thompson [46]. The model was not applied in the simulation presented here in this dissertation, because it only describes the evolution of mechanical stress, and

$l/l_e<1$, $l/l_s<1$ Diffusion dominated	$l/l_e>1$, $l/l_s<1$ EM dominated
$l/l_e<1$, $l/l_s>1$ Vacancy production dominated	$l/l_e>1$, $l/l_s>1$ Mixed case

Figure 4.1: Four general cases for the Kirchheim model are displayed: diffusion dominated (case I), vacancy production dominated (case II), EM dominated (case III), and a mixed case.

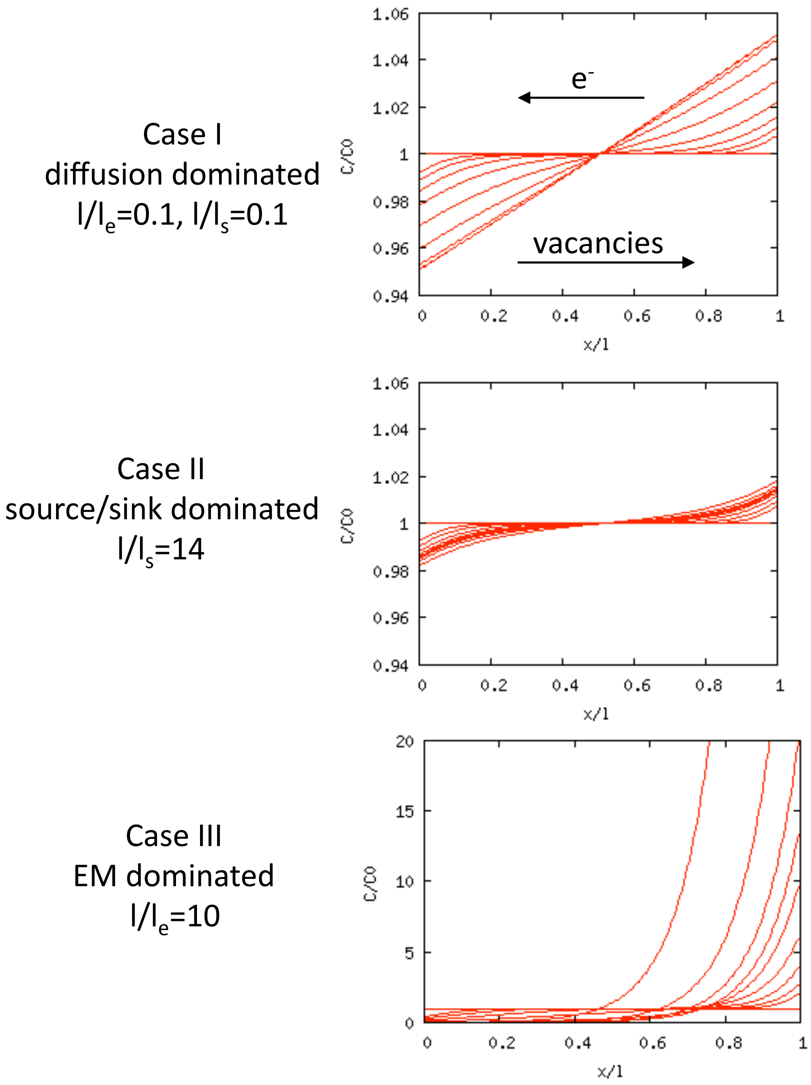


Figure 4.2: Numerical solutions of the Kirchheim equations. Case I, case II and case III are the diffusion dominated, source/sink dominated and the EM dominated cases, respectively. The curves are displayed at reduced time θ=0.005, 0.01, 0.02, 0.04, 0.08, 0.15, 0.3, 0.6 and 1.2.

not the accumulation of vacancies, which is pertinent for the void nucleation and growth model described in this dissertation. Nevertheless, the Korhonen model is very popular, which is why the derivation is included as follows.
Equation 4.12 shows the driving forces for electromigration.

$$F = \Omega \frac{d\sigma}{dx} + Eq^* \tag{4.12}$$

where the left term of the right hand side of the equation relates to the mechanical stress driving force and the right term to the electromigration driving force. Ω, σ, E and q^* stand for atomic volume, mechanical stress, electric field and effective charge, respectively.
Equation 4.13 relates the atomic flux j to the particle velocity v and atomic concentration C_a.

$$j = vC_a \tag{4.13}$$

The particle velocity v is given as the product of the mobility μ and the driving force F, as shown in equation 4.14.

$$v = \mu F \tag{4.14}$$

Thus, the flux j can be written as

$$j = \mu F C_a \tag{4.15}$$

With regard to the Einstein relation, the mobility can also be written as

$$\mu = \frac{D}{k_B T} \tag{4.16}$$

where D is the diffusivity, k the Boltzmann constant and T the temperature. Substituting Equation 4.16 and 4.12 into 4.15, the result is

$$j = \frac{D}{kT}\left(\Omega\frac{d\sigma}{dx} + Eq^*\right)C_a \tag{4.17}$$

The continuity equation

$$divj = -\frac{dC}{dt} \tag{4.18}$$

takes the following form for one dimension:

$$\frac{dj}{dx} = -\frac{dC}{dt} \tag{4.19}$$

Equation 4.20 is the confinement relation, which is the most important in the Korhonen model. It means that a relative atomic concentration change leads to a buildup of mechanical stress inversely proportional to the bulk modulus B of the confining embedment of the metal line.

$$\frac{dC_a}{C_a} = -\frac{d\sigma}{B} \tag{4.20}$$

Within the range of linear elasticity, the atomic concentration C_a can be viewed as constant, set to the inverse of the atomic volume Ω as seen in equation 4.21.

$$C_a = \frac{1}{\Omega} \tag{4.21}$$

Substituting Equation 4.21 in 4.20, one gets

$$dC_a = -\frac{d\sigma}{B\Omega} \tag{4.22}$$

Further substitution of equation 4.22 in 4.19 yields

$$\frac{\partial j}{\partial x} = \frac{1}{B\Omega}\frac{d\sigma}{dt} \tag{4.23}$$

After a final substitution of Equation 4.17 in 4.23 and keeping in mind Equation 4.21, the result is

$$\frac{\partial}{\partial x}\left[\frac{D}{k_B T}\left(\frac{d\sigma}{dx}+\frac{Eq^*}{\Omega}\right)\right]=\frac{1}{B\Omega}\frac{d\sigma}{dt} \tag{4.24}$$

which is equivalent to

$$\frac{\partial\sigma}{\partial t}=\frac{\partial}{\partial x}\left[\frac{DB\Omega}{k_B T}\left(\frac{d\sigma}{dx}+\frac{Eq^*}{\Omega}\right)\right] \tag{4.25}$$

Equation 4.25 can be made more compact by setting $\kappa = DB\Omega/k_B T$ and $\gamma = Eq^*/\Omega$, which yields the Korhonen relation for mechanical stress evolution in metal lines for one dimension (equation 4.26).

$$\frac{\partial\sigma}{\partial t}=\frac{\partial}{\partial x}\left[\kappa\left(\frac{d\sigma}{dx}+\gamma\right)\right] \tag{4.26}$$

Notice that for constant κ and γ the Korhonen relation takes the form of the diffusion equation.

With the Korhonen model, the mechanical stress evolution can be calculated for one dimension. As mentioned above, the Korhonen model was presented, because of its popularity. The model does not cover the evolution of vacancy concentration, which is pertinent to the void nucleation and growth model developed in this work. Therefore, the Korhonen model was not applied in this dissertation.

4.1.3.1 Application of Korhonen's model : MIT/Emsim

MIT/Emsim is an electromigration simulator for one-dimensional interconnects based on the Korhonen model [46, 45], developed at the Massachusetts Institute of Technology in the group of C. V. Thompson. Dependent on current density and temperature, the atomic fluxes and the stress evolution in an interconnect is calculated. The simulator was extended to handle interconnect trees.

4.1.4 FEM Modeling Approaches

Sukharev et al. have published numerous works, treating electromigration simulation in dual-inlaid interconnects of integrated circuits with the finite element method (FEM) [47, 48, 49, 50, 51, 52, 53, 54, 55]. Sukharev's theoretical approach builds onto the work of Rzepka [56]. In his physical model, Sukharev includes all important driving forces into the mass balance equation, including electromigration and stress gradient driving forces.

Other examples of FEM simulations are those from the Bower group [57, 58, 59] and from Ceric et al. [60, 61, 62, 22].

For simplicity considerations, FEM tools were not used in this dissertation. The employed finite difference method is based solely on the development of software by the author with emphasis on not using any foreign software. The modeling of void nucleation and growth as done in this dissertation is more convenient on a finite difference lattice than it would be on an finite element mesh.

4.1.5 Monte Carlo Modeling Approaches

An interesting approach was made by Bruschi et al. [63] using an atomistic Monte Carlo technique to model electromigration. A similar approach was made during the work of this dissertation, placing atoms in the cell network representing the grain boundaries. The cells exchanged atoms at a specific probabilistic rate due to diffusion, while the diffusion probability in the direction of electron flow was set higher. Thus, a net motion of atoms due to electromigration was achieved. Although interesting, the approach posed a major problem of how to convert the electric current density to diffusion probabilities. The programming was done collaterally and the development of the algorithm did not reach a stage where it could replace the finite difference model of this dissertation due to the stated problem. The approach is not further documented here.

Other examples of Monte Carlo techniques to specifically model the motion of voids can be found in References [64, 65].

4.1.6 The Model used in this Dissertation

The model used in this work describes the transport of vacancies. Generally, the flux of the vacancies can be expressed as concentration times velocity, as shown in equation 4.27.

$$\mathbf{j} = \mathbf{v} C_v \tag{4.27}$$

Equation 4.27 is derived from Equation 4.13, except for the fact that here vacancies are observed.

The velocity of the vacancies is given as $v = \mu F$. Keeping in mind the Einstein relation $\mu = D/kT$ and the driving forces from 4.12 one obtains the following equation:

$$\mathbf{j} = C_v \frac{D}{kT} \left(Z^* e \rho \mathbf{j_{el}} - f \frac{\Omega}{N_A} \nabla \sigma \right) \tag{4.28}$$

where $Z^* e = q^*$ and $\rho j_{el} = E$ were substituted in equation 4.12 and the one-dimensional $d\sigma/dx$ was replaced by the gradient of the stress ($\nabla\sigma$). Z^* is the effective charge number, j_{el} the electric current density and N_A Avogadro's number. Due to numerical complications regarding the implementation of mechanical stress, the implementation was relinquished. Therefore, Equation 4.28 simplifies to

$$\mathbf{j} = C_v \frac{D}{kT} Z^* e \rho \mathbf{j_{el}}. \tag{4.29}$$

For one dimension, the equation can be written as

$$j = C_v \frac{D}{kT} Z^* e \rho j_{el}. \tag{4.30}$$

Including the Fick diffusion term, Equation 4.30 becomes

$$j = -\frac{dC_v}{dx} + C_v \frac{D}{kT} Z^* e \rho j_{el}. \tag{4.31}$$

For simplicity, the vacancy concentration C_v will be written as C:

$$j = -\frac{dC}{dx} + C \frac{D}{kT} Z^* e \rho j_{el}. \tag{4.32}$$

Figure 4.3 shows the discretization lattice of the partial computation domain with the cell (i,k) in the center for which the computation of the flux shall be demonstrated. The total flux is computed as the amount of material entering

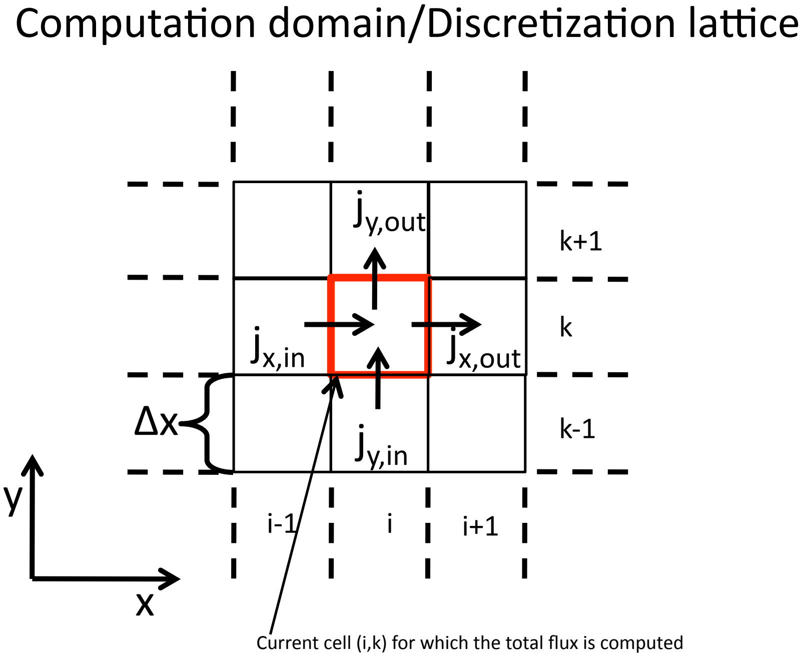


Figure 4.3: Illustration of the total flux computation for a discretization lattice cell.

the left side ($j_{x,in}$) minus the amount of material exiting the right side ($j_{x,out}$) plus the material entering from the bottom ($j_{y,in}$) minus the material exiting at the top ($j_{y,out}$). Using Equation 4.32, $j_{x,in}$ can be written in discretized form as

$$j_{x,in} = -\frac{C_{i,k} - C_{i-1,k}}{\Delta x} + C_{i-1,k}\frac{D_{i-1,k} + D_{i,k}}{2kT} Z^* e\rho j_{el}. \tag{4.33}$$

The other three fluxes $j_{x,out}$, $j_{y,in}$ and $j_{y,out}$ will be calculated analogously. The total flux j_{total} is calculated as mentioned as

$$j_{total} = j_{x,in} - j_{x,out} + j_{y,in} - j_{y,out}. \tag{4.34}$$

The flux must fulfill the continuity Equation 4.35.

$$div\mathbf{j} = -\frac{dC_v}{dt} \tag{4.35}$$

In one dimension, Equation 4.35 is written as

$$\frac{dj}{dx} = -\frac{dC}{dt}. \tag{4.36}$$

In discretized form, the vacancy concentration of cell (i,k) $C_{i,k}^{n+1}$ for the time step n+1 can be written using Equation 4.36 as

$$C_{i,k}^{n+1} = C_{i,k}^{n} + \frac{j_{total}}{\Delta x}\Delta t. \tag{4.37}$$

With Equation 4.37, the evolution of vacancy concentration can be calculated for the entire computational domain. The method in Equation 4.37 of adding the product of the discrete flux derivative ($j_{total}/\Delta x$) and Δt to the current value of concentration is known as the forward-Euler method. The forward-Euler method is a numerical method for solving ordinary differential equations with initial values, and this procedure is the most basic kind. The partial differential equation of the flux, which basically is a diffusion equation, was transformed into a more simple difference equation (4.37), which is not different from a difference equation based on an ordinary differential equation. The forward-Euler method was applied due to the similarity of the problem to an ordinary differential equation.

4.2 Electromigration Simulation Procedure

Figure 4.4 displays a flowchart of the simulation procedure. In the beginning of the simulation, the microstructure is generated using the Monte Carlo technique of the modified Potts model. The simulation time is set to t=0 and the electromigration mass transport modeling starts. While the voids grow, the electrical resistance of the simulated interconnect segment is recorded for every time step. When a previously set time step is reached, the simulation ends.

The simulation is two-dimensional and treats only line segments of the interconnect, no via structures.

At first, several (typically 100) interconnect segments are generated in such a way that they contain a microstructure. The generation takes place with a Monte Carlo technique using a modified Potts model. The grain size is determined by the number of Monte Carlo steps. The size of the segments was typically 300 pixels in length and 100 pixels in height. The calibration was set

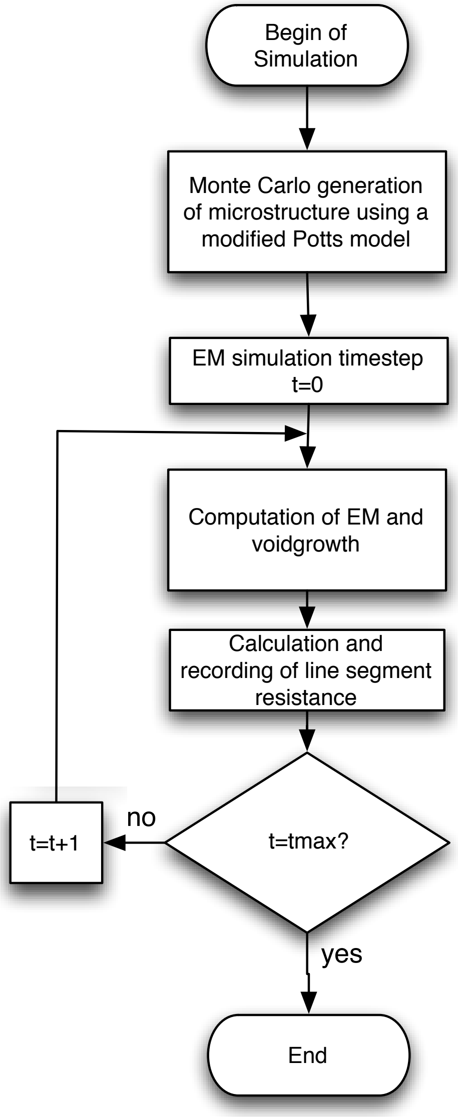


Figure 4.4: Electromigration simulation flowchart

to 1 nm per pixel so that the segment is 100 nm in height, which is reasonable. The next step that the program operating on one segment has to handle is the determination of the grain boundaries. For that, the energy in terms of the Monte Carlo grain growth technique is calculated for each lattice site. In false colors, this energy is the number of differently colored neighbors that the site has, where the grains all have distinct colors. The false colors are a qualitative measure for the crystallographic orientation of the grains. The neighbors of the orthogonal lattice are the four nearest neighbors to the left, right, top and bottom plus the four diagonal ones (second nearest neighbors). When the energy is larger than zero, the site is interpreted as belonging to a grain boundary. In contrast, when the energy is zero, which means that all surrounding colors are identical, the site is located inside the grain (or the bulk). The number of all lattice sites with energy larger than zero comprise the grain boundaries.

4.2.1 Setting The Diffusion Constants

On the one hand, the grain boundaries are diffusion paths, and on the other hand - to implement the top interface - the first upper lattice line is a diffusion path as well (interface). A diffusivity matrix is created, which is symmetric. This matrix establishes the diffusivity in multiples of a base diffusivity for the grain boundaries. The columns and rows specify the orientation (color) of the two grains participating in a boundary point (site). If there are more than two grains, the second grain is randomly chosen. If the two grain colors are identical, which means that the lattice site is not located at a boundary (it is in the bulk), the diffusivity is set to zero, because the bulk diffusion is neglected. This fact is expressed by a diagonal of zeros in the matrix. If the two grains are switched, the diffusivity remains unaffected, which is why the matrix is symmetric. The off-diagonal elements are filled with positive random integers in a specified range, e.g. from 100 to 150.

The values are chosen randomly, because only little information is available that clarifies the different diffusion properties for all the specific grain orientations. The diffusivity is a function of grain orientation and diffusion direction as well as the combination of participating orientations in a grain boundary. Since it is impossible to gain all that information from measurements and since the grain orientations are only available qualitatively in the simulation, the diffusivity factors are chosen randomly. This assumption is justified, because the goal of the simulation is to reflect the variation in diffusivities that lead to flux divergent sites rather than an exact modeling of the diffusion properties.

Table 4.1 shows selected activation energies of Cu self-diffusion along different Cu surface orientations. The table demonstrates the varying nature of diffusion properties in dependence of crystallographic orientation. Similarly to the chosen orientations along the Cu(111), Cu(100), Cu(110) surfaces with activation energies of 0.04, 0.28-0.40, 0.35/0.84 eV [66, 67, 68, 69], respectively, the diffusion properties vary for all possible surfaces and directions present in an interconnect microstructure. The spread in activation energies in Table

4.1 is remarkable, especially the low value of 40 meV for the (111) surface, which is an activation energy comparable to liquid. Nevertheless, this number of 40 meV was found by evaluation of the jumping frequencies of Cu atoms in a scanning tunneling microscope (STM) [67]. It would be a tremendous endeavor to measure and know all the activation energies for all possible combinations and to model these in the simulation, which is at least at present, not possible. This is why the diffusion constants were assigned randomly in the simulation.

In addition to the matrix, a vector is created for the diffusion factors of the interface. The vector is as long as there are different grain orientations (inherently 30 from the Monte Carlo grain growth). The vector contains random values as does the diffusivity matrix. The range of the values is generally different than that of the matrix to reflect its different diffusion condition compared to the grain boundaries. After setting up diffusion matrix and vector, the diffusivity factors are mapped onto the two-dimensional interconnect segment model. It should be pointed out that in this simulation the interface and grain

Cu surface	Direction	Activation energy (eV)	Reference
(111)		0.04	[66, 67]
(100)		0.28-0.40	[66, 68]
(110)	(1-10)	0.35	[66, 69]
(110)	(001)	0.84	[66, 69]

Table 4.1: Experimentally measured activation energies of Cu self-diffusion along different crystallographic orientations (surface diffusion) to demonstrate the varying nature

boundaries are 1 nm and 2 nm thick, respectively (using the calibration of 1 nm referring to 1 per lattice site).

4.2.2 Mass Transport

The next step is the modeling of the electromigration mass transport as well as the void formation and growth. In this simulation, the transport of vacancies is considered rather than the transport of atoms. For this, an additional map (in addition to the diffusivities) is created that contains the number of vacancies. The atomic volume was chosen to be 10^{-5} m^3/mol and the number of vacancies was set to 20 at.%. This initial vacancy concentration is unreasonably high, but it was chosen to make voiding happen in less amount of computation time. The high number of vacancy concentration was also used by Kirchheim in his model for the same reason [44]. The accurate atomic volume of Cu is 7.1× 10^{-6} m^3/mol, but 10^{-5} m^3/mol was chosen for computational convenience. Thus, the initial concentration of vacancies is 20,000 mol/m^3. This value is assigned to every lattice site in the map of the segment. An electric current is applied. The magnitude of the current was set to 10^{14} A/m^2, which is larger by a factor of 1000 from already high experimental test current densities of 10^{11} A/m^2 = 10 MA/cm^2. The reason for this is to yield voiding in a smaller amount of computation time. Despite the elevated current density, the temperature was held at 300°C. The simulation time step was chosen to be $\Delta t = r * \frac{\Delta x^2}{D_{base}}$, where r is the integration constant set to 0.0001, Δx is the smallest length (length of a cell edge) and D_{base} is the base diffusion constant. The formula for Δt with r=0.0001 was found empirically to guarantee that the computation remains stable. Δt is in the range of microseconds, much smaller compared to the usual electromigration testing lifetimes measured in hours. To overcome the time window incompatibility between diffusion (microseconds) and electromigration (hours), the electric current was chosen to be extremely high. The maximum time step computed with this simulation was 5,000,000, which corresponds to a few seconds in real time. Setting the electric current to 10^{14} A/m^2 contracts the electromigration lifetimes of the segments to the range of seconds, which is comparable with the total real time. In this simulation, the variation of current densities, e.g. around voids, was not calculated. The current density is constant across the whole interconnect segment. Hence, such effects like current crowding cannot be taken into account.

With the applied current, the flux of vacancies is calculated between all the cells (pixels) of the segment, in particular, the flux from the left of the cell, to the right, from the bottom and to the top. A finite difference scheme is applied with dx as the step width between the cells. The divergence of the flux corresponds to a change in vacancy concentration per time. In this numerical scheme, the divergence of the flux is approximately calculated as the sum of the differences between right and left, top and bottom flux, divided by the mesh constant dx. The approximate flux divergence is multiplied by the time step Δt to yield the vacancy concentration change. The change is then added up to the existing vacancy concentration in the cell. The evolution of vacancy concentration in every cell is calculated.

Figure 4.5 shows the flux of vacancies at a grain boundary triple point at a

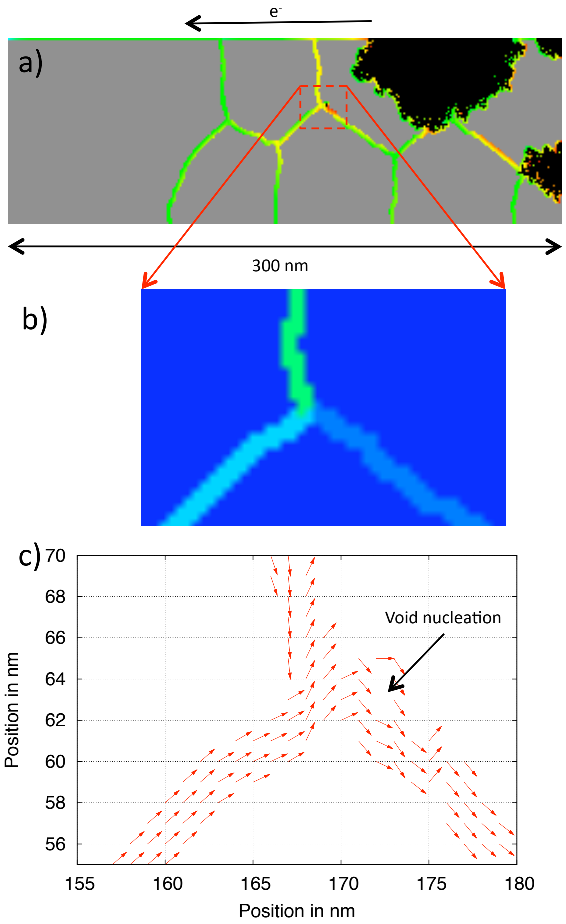


Figure 4.5: (a) Vacancy concentration map - red and blue mean high and low concentration, respectively, voids are black and the inside of grains are gray. (b) Diffusivity map of the dashed region of (a), on a scale from blue to red, the diffusivity increases. (c) Flux vector plot of the void nucleation site (dashed region of (a)).

selected area of interest. In Figure 4.5a the modeled interconnect segment is shown. The insides of grains are drawn in gray and the grain boundaries are colored according to the vacancy concentration, where the color green points to low vacancy concentration and the color red to high concentration. Voids are drawn in black. The electron flow direction is from the right side to the left side of the image. Inside the interconnect segment, a grain boundary triple point and the surrounding area is selected as the area of interest (dashed rectangle). Figure 4.5b shows the diffusion properties for the selected area of interest. The diffusion constant is mapped with an RGB color scale, where the diffusion constant increases from blue to red. However, the color red is not shown, because the range of the diffusion constants extends only to green. The main area around the grain boundary triple point is colored in dark blue, which means that the diffusion constant is set to 0. This fact reflects the characteristic that the diffusion inside the grains is neglected. The lighter blue color of the grain boundary pointing to the lower right corner of the clip shows a diffusion constant above 0 and the grain boundary in light blue color pointing to the lower left shows a higher diffusion constant. The vertical grain boundary in the middle upper field of the corner (green) has the highest diffusivity, although no electromigration flux is to be expected along this grain boundary because it is oriented perpendicular to the electron flow. Overall, the grain boundary from the lower left corner of the clip should transport more vacancies to the grain boundary triple point than the grain boundary pointing to the lower right transports away from the triple point. The upper middle vertical grain boundary transport can be neglected, because of the perpendicular orientation to the electron flow, as mentioned above. Thus, the grain boundary triple point is a flux divergent site and void nucleation is to be expected. Figure 4.5c shows the vacancy flux along the grain boundaries of the selected area of interest. It can be seen that vacancies are transported from the lower left to the triple point and from the triple point to the lower right of the clip. The flux along the vertical grain boundary segment is not well defined, as expected. What cannot be clearly seen is that the left grain boundary transport is slightly larger than the right grain boundary transport, although this can be assumed by the diffusion properties from Figure 4.5b. Finally, a pointer in Figure 4.5c marks the location of the void nucleation. It is not well understood why the location of the void nucleation is slightly off the center to the right from the triple point.

4.2.3 Finding a suitable void growth algorithm

When the vacancy concentration of a cell reaches a threshold, e.g. 30,000 mol/m^3, and none of the surrounding cells is a void yet, a void nucleates and the cell is declared void. If a surrounding cell - meaning left, right, top, bottom and the cells on the diagonals - is a void cell already, then the void growth mode is applied. Many different algorithms have been developed and tested. The simplest one is making any cell void where the vacancy concentration threshold is reached, without making the distinction that a neighboring cell is void. The application of this void growth mode led to undesired results. The voids grew long and in zig-zag shape, oriented in the direction of current flow. The small diameter of these zig-zag tubes (or nano-kinks) was one cell. The amplitude of the zig-zags was three cells (Figure 4.9). A different solution needed to be found. After trial-and-error, a random-based void growth algorithm was found to be the most useful.

4.2.3.1 The random-based void growth algorithm

The random-based void growth algorithm works in the following way. Assuming that the concentration of a cell reached the threshold and that this cell has a neighbor cell that is void, then the cell that has reached the threshold shall be called the void candidate. Now the surface of the void cell will be determined. All the non-void neighbors of the void cell are counted as the surface. Then one of the non-void neighbor surface cells is randomly selected and declared void, instead of the void candidate. The concentrations of the void candidate and the randomly chosen cell are switched. In case that the void candidate borders a cluster of cells, the cluster and its surface is determined and a cell to be declared void is chosen from the surface. This procedure ensures that the void grows round, although the surface can become very rough, which is tolerated. The switching of the vacancy concentrations can be interpreted as a fast diffusion step. The switching is necessary, because in the next cycle (time step) of traversing the segment cells to search for exceeded thresholds, the former void candidate would be flagged again as new candidate since its concentration is still above the threshold. The void would grow without necessary vacancy transport.

4.2.4 Interconnect Resistance Calculation

The void growth algorithm is applied after each time step. With growing voids, the electrical resistance of the segment increases. The resistance is calculated and monitored. The segment is divided in rows and columns of cells. For the resistance calculation, the layer of rows times columns is extended by a layer representing the Ta shunt layer. Since only a qualitative measure of the resistance is required, the Ta layer cells have the same dimensions as the Cu cells. The cells are regarded as cubes with a side length of 1 nm, according the calibration of 1 pixel equals 1 nm. First the copper cells (those that are non-void) in a column are counted and the resistance is calculated as if the cells were contiguous. The resistivity of Cu and Ta was set to 1.7×10^{-8} Ωm (pure Cu at room temperature) and 2.0×10^{-7} Ωm (α-Ta), respectively. Actual numbers may very for different implementations and companies due to the fact that not only pure Cu and α-Ta are used. The emphasis is, however, on obtaining a qualitative measure for the line resistance. The time-to-fail is generally when the whole height of the interconnect is depleted and does not depend on the actual specific number for the resistivity. The main reason to incorporate a shunt layer into the calculation is to prevent an open circuit when a whole column becomes void. The resistance of one column is calculated in parallel from the resistance of the Cu column and the extended Ta cell. The resistance of the whole interconnect segment is calculated as series of the resistance of the columns. In this way, a measure for the segment resistance is obtained. Calculating the resistance as a series of parallel vertical cells is a very simplified model, and it is not physically exact. Nevertheless, the method delivers a useful qualitative measure.

4.2.5 Finding a Suitable Failure Criterion

During the void growth simulation, the resistance is recorded. After the simulation, collecting all the data from the parallel computer processors, the resistance curves are evaluated. A measure of 400% resistance increase, or 5 times relative resistance increase, for an interconnect segment fail criterion proved to be practicable. This measure was derived by observing many resistance curves obtained by the simulation. The beginning of the curves showed slow, non-linear increases, which can be attributed to void formation. The slow increases were followed by steep jumps, which can be explained as the voids growing to the full height of the segments, leaving only the shunt layer. Almost all the curves revealed the switch from slow first increase to steep jumps just below the 400% mark, which is why the criterion was chosen. The criterion is much higher from the typical 10% resistance increase for a line to fail in physical experiments. The reason is that in physical experiments, the lines are much longer (up to and several 100 um). In the simulation, the interconnect segments are usually 300 nm long. The void growing to the full height (100 nm) of the segment in the simulation fills approximately 1/3 of the segment, while a similar void in a 100 um long line (and 100 nm in height) fills 1/1000 of the line. Therefore, the relative resistance of the short segment rises much faster than that of the long line. Also, the switch from the slow increase to the steep jump occurs at a higher relative resistance, justifying the high fail criterion of 400%.

Figure 4.6 shows an example resistance trace with corresponding void growth snapshots at special marks. Mark A points to the first significant resistance increase, which is characterized by a depletion of material across the full height of the interconnect segment. Between mark A and B, the layer of residual material at the bottom of the lower interconnect segment area at the right corner is continuously depleted, extending the empty region with a full height removal. Between mark B and C, the residual layer of material at the bottom of the interconnect segment area is thinned, without extending the full height empty region, which is characterized a smaller slope of the resistance trace compared to the interval between A and B. Between mark C and D the slope of the trace increases again, because the void area "touches down" at a second location at the bottom of the interconnect segment. It is to be noted that at the bottom a shunt layer is modeled, which is invisible in the snapshots and corresponds to the Ta-based barrier layer of real interconnects. This shunt layer carries the electric current at regions where the interconnect segment is depleted to the full height. The shunt layer is the reason why the electrical resistance does not go up to infinity. From mark D on the resistance increases with a slightly smaller slope until the end of the simulation. The final void continues to grow larger, at a slightly lesser rate than the thinning of the previous residual layer of material at the bottom of the interconnect segment.

Figure 4.7 shows an enlarged view of Figure 4.6 at the region of mark A, with additionally marked snapshot sites E and F. Mark F shows the location of the resistance trace where the slope starts to pick up. According to the snapshot, this behavior occurs shortly before a full height of the interconnect segment is depleted. Mark E points to the threshold of the chosen failure criterion of 400% (5 times the initial value). The corresponding snapshot clearly shows that the full height of the interconnect segment has been depleted at the right hand side of the clip. This circumstance justifies the choice of the 400% resistance increase failure criterion. The characteristics of the resistance trace is inconsistent compared with the resistance traces of real electromigration testing experiments. In physical experiments, typical resistance increase failure criteria range from a few percent to 10 or 20%. The reason why the criterion for the simulation is that much higher is the fact that the interconnect segments in the model are so much shorter (300 nm compared to several hundred micrometers).

Figure 4.8a shows the resistance traces for a simulation of electromigration for 100 different interconnect segment microstructure configurations. After an initial resistance increase the resistances increase with more or less comparable slopes until the end of the simulation run. The slopes after the initial significant resistance increase correspond to the steady growth of the final voids. Figure 4.8b shows an enlarged view of the traces at the first resistance increase. The dashed line corresponds to the failure criterion threshold. The dashed line intersects almost all the traces after the first resistance jump, further justifying the choice of the 400% resistance failure criterion.

4.2.6 Summary

To summarize, the simulation was started on many computer processors. Firstly, each processor generated a microstructure for an interconnect segment (typically 300x100 nm^2). As a second step, the diffusivity factors were applied to the grain boundaries and to the upper cell line (which represents the top interface). With a finite difference scheme, the transport of vacancies was

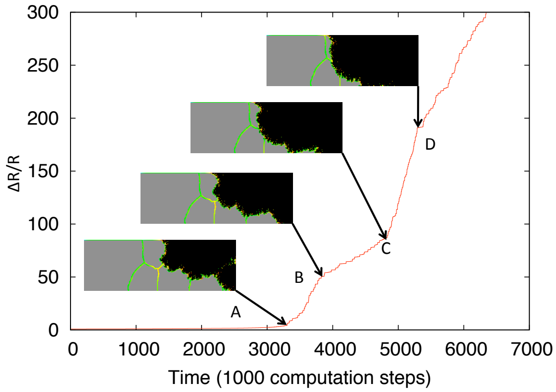


Figure 4.6: Sample resistance trace with corresponding void growth snapshots at special marks.

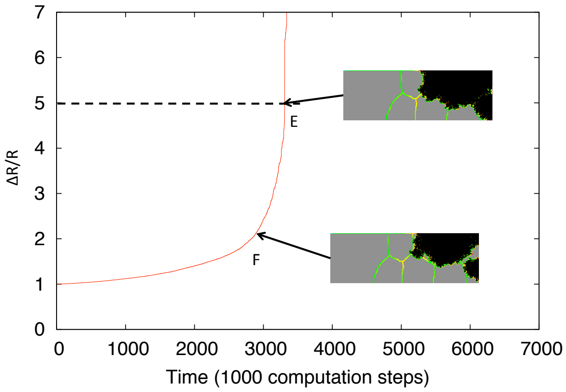


Figure 4.7: Enlarged view of the resistance trace from Figure 4.6 at the first resistance increase.

modeled. At flux divergent sites, where vacancies accumulated and where the concentration of vacancies reached the threshold (25,000 mol/m3), a void was nucleated. The growth of voids was treated with a random-based algorithm. During the void growth simulation, the electrical resistance was monitored. A shunt layer was placed at the bottom of the interconnect segment to prevent an open circuit in case a void grows to the full height of the segment. After the simulation, a fail criterion of 400% resistance increase was applied to the recorded resistance curves of all the processors. The lifetimes can be further manipulated in a statistical analysis.

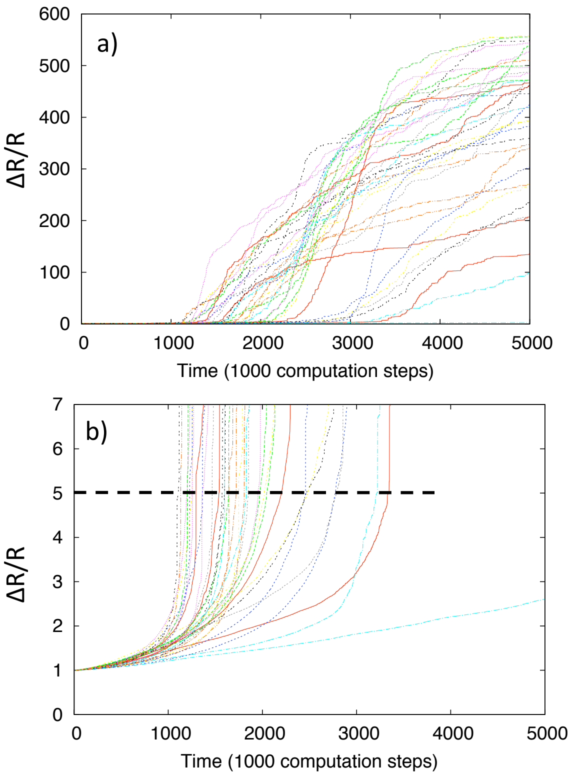


Figure 4.8: Electrical resistance traces for the electromigration simulation for 100 different interconnect segment microstructure configurations. a) full view. b) enlarged view to show the behavior of the first resistance increase. The dashed line is the chosen failure criterion of 400% resistance increase (5 times the initial value).

4.3 Simulation Parameters

Property	Value	Reference
Current density j_{el}	10^{14} A/m^2	
δD_{GB} in m^3/s	5×10^{-15}	[70, 71]
D_0 in m^2/s	10^{-5}	
Temperature T in $°C$	300	
Activation energy Q in kJ/mol	104	[70, 71]
D_{base} in m^2/s at 300 $°C$	3.33×10^{-15}	
Z^*	3.5	

Table 4.2: Constants used in the simulation.

4.4 Electromigration Simulation Results

The first result is depicted in Figure 4.9. It shows a 300x100nm^2 piece of an interconnect model, for which the degradation process of electromigration was simulated. One can see the copper grains (gray) and the diffusion paths (colored). In terms of diffusion paths, blue means a low vacancy concentration and red means a high concentration. The boundary conditions of this simulation model are chosen such that the anode end (left) as well as the cathode end (right) are diffusion barriers. One can observe clearly the void growth at the cathode end (black). The so-called void growth model "Free" was applied.

For the void growth model "Free" a volume element is declared void element if the vacancy concentration transcends a certain threshold. In Figure 4.9 the vacancy concentration threshold is 25000 mol/m^3

Additionally one can see in Figure 4.9 zig-zag artifacts, which grow from the diffusion paths into the copper grains in the opposite direction of the electron current flow. These artifacts are formed because of the discretization and the choice of the algorithm. Figure 4.10 shows an attempt to eliminate the zig-zag structures by increasing the vacancy concentration threshold to 30000 mol/m^3. The artifacts disappeared down to two jags, but the result is still not satisfactory. As a consequence, the void growth model "Free3" was written.

For the void growth model "Free3" two criteria have to be fulfilled for the declaration of a volume element as void element. Firstly, as for the model "Free", a vacancy concentration threshold must me reached. Secondly, a void element candidate needs at least three void elements as neighbors. This idea formed because its application avoids zig-zag structures, and a void can grow more compact. Figure 4.11 shows the result of the application of the void growth model "Free3". As can be observed, the zig-zag structures are removed, but rudiments remain. The long stretched voids at the anode end can be interpreted as remnants of the zig-zag structures. A bit of the zig-zag formation is still visible. The diameter of the long stretched voids are three volume elements, as opposed to one volume element in the zig-zag structures of Figure 4.9 (void growth model "Free").

The diffusivity for the calculation for Figures 4.9 to 4.11 was constant for all diffusion paths. The diffusivity constant corresponds to a reference grain boundary diffusion constant of D_{base}. To arrange for a more realistic simulation, a non-constant diffusivity was applied for the following calculations. Since the grain boundaries generally exhibit different diffusivities, depending on the crystallographic orientation of neighboring grains, and only some experimental results are available, the diffusivities where generated randomly. Multiples of the reference diffusivity D$_{base}$ were distributed statistically on the grain boundaries. Figure 4.12 shows the relative diffusivities. Blue corresponds to 0 and red to the 10-fold of D$_{base}$. With this preference, the calculations for Figure 4.11 were repeated and the result is shown in Figure 4.13. The long stretched voids growing into the grains are still visible. The number of the long stretched voids increased compared to Figure 4.11. The long stretched voids depict a computationally undesired form of void growth. Additionally, empty boxes are visible at the upper interface, that typically have a width of three volume elements. To be declared void in the void growth model "Free3", the minimal number of neighboring void cells for the void candidate was three. That means the three and less void elements correspond to the formation of voids and more than three void elements correspond to the growth of voids. Thus, a mini cluster of three void elements must form in order to apply the void growth model "Free3". Apparently, the void formation is favored at the upper interface, but the growth of voids is suppressed in the algorithm. Therefore, voids grew with a width of three elements.

The result is not satisfactory and it was attempted to improve the void growth. One criterion should be fulfilled: the voids must grow compact, centered and not long stretched or in zig-zag structures. One solution is the void growth model "Random". A void will grow by one void element in the following way: the void element is selected randomly from the void surface. This procedure ensures a compact and centered growth, because there is no preferred direction of growth. Figure 4.14 shows the result of the application of the void growth model ”Random”. One can observe multiple voids that are centered at their origin. A disadvantage is the rough surface of the voids. Comparing the approximate location of the void centers with the diffusivity map in Figure 4.12, it can be seen that most voids are located at sites of jumps of the diffusivity constant. These jumps cause flux divergencies. The appearance of voids at sites of flux divergencies supports the legitimacy of the simulation.

Observing the longer stretched void at the middle of the upper interface, the void growth model was developed further. The growth void element from the surface was chosen in such a way that the choice of an element with a higher number of void neighbors is more probable. Such an approach will accomplish that voids continue to grow at sites with the highest number of void neighbors. The result of this ”Random/void-weighted” model is shown in Figure 4.15. As can be seen, the longer stretched void in Figure 4.14 now appears centered as well.

All of the calculations were carried out in two dimensions with a resolution of 300x100 units^2, where one unit corresponds to 1 nm.

Figure 4.16 shows an image sequence of void growth using the “Random” model. The electron flow is from the right to the left side of the images. As in the previous figures, the insides of grains are drawn in gray and the grain boundaries are colored corresponding to the vacancy concentration, with a RGB color scale where blue is low and red refers to high vacancy concentration. The color blue does not appear in the grain boundaries, because there

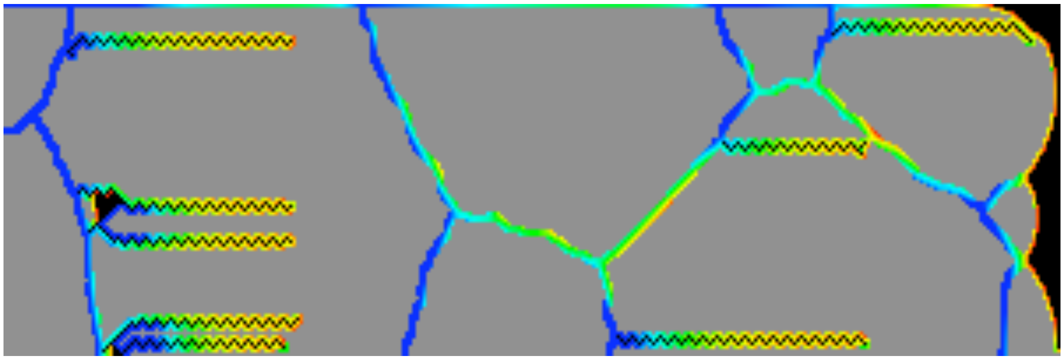


Figure 4.9: 100×300 nm^2 interconnect segment (2D). The cathode is on the right hand side and the anode on the left. The zig-zag structures are simulation artifacts. The void nucleation threshold was set to 30000 mol/m^3 vacancy concentration. The Cu grains (gray), the diffusion paths (colored) and the cathode voiding (black) are shown. Red means high vacancy concentration and blue low. The applied void growth model is "Free". Cathode and anode are diffusion barriers.

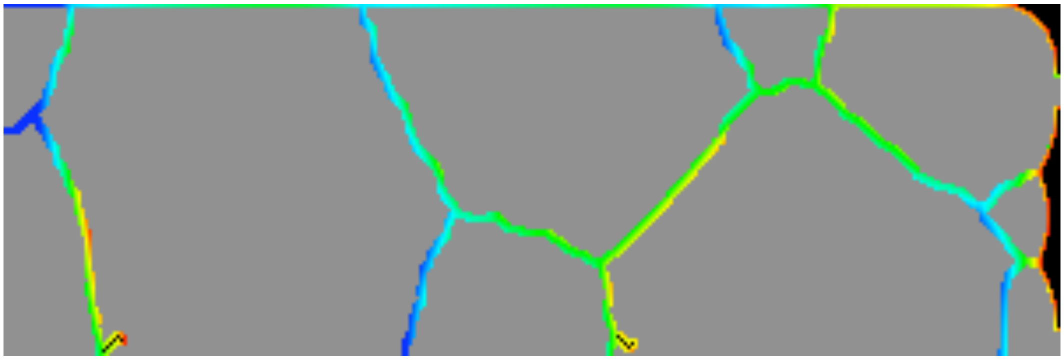


Figure 4.10: As in Figure 4.9 but with a vacancy concentration threshold of 35000 mol/m^3. Almost all of the zig-zag structures can be suppressed.

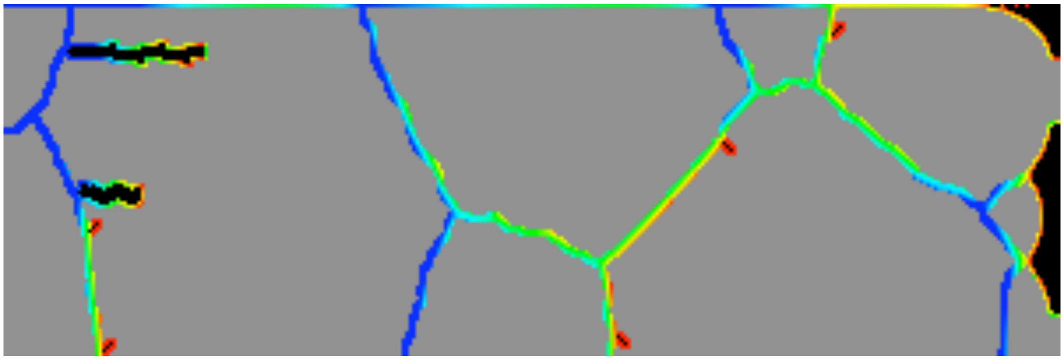


Figure 4.11: As in Figure 4.9 and 4.10 but with void growth model ”Free3”. The vacancy concentration threshold was set to 25000 mol/m^3.

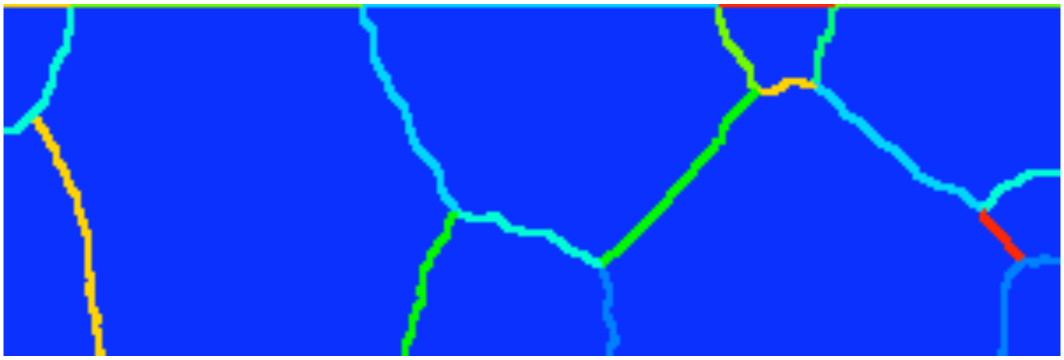


Figure 4.12: 100×300 nm^2 interconnect piece. The relative diffusivity is shown. Blue corresponds to 0 and red corresponds to 10 times the minimum grain boundary diffusivity.

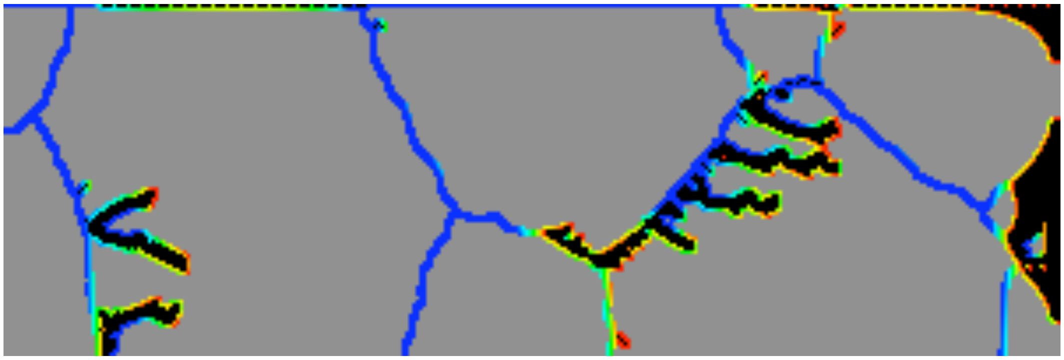


Figure 4.13: 100×300 nm^2 interconnect piece. As in Figure 4.11, but with applied diffusivity as shown in Figure 4.12. Artifact formation is clearly visible: empty cells at the top interface and branches growing inside the grains.

Figure 4.14: 100×300 nm^2 interconnect segment. As in Figure 4.13, but with applied void growth model "Random". Void growth is centered around the void origin except for the long void at the top interface.

are no grain boundary sections with such low vacancy concentration. Figure 4.16a shows the initial microstructure. There are three vertical grain boundaries in the upper half of the image and one horizontal grain boundary pointing to the right end of the image. In Figure 4.16b exhibits the formation of the initial voids. There is one void visible at the top of the right most previously mentioned vertical boundaries. The void started at the intersection of the top interface with the grain boundary, which is plausible. Neglecting the transport along the vertical grain boundary segment, because it is oriented perpendicular to the electron flow, the left segment of the top interface adjacent to the void must transport more vacancies opposite to the electron current flow than the right segment of the top interface adjacent to the void. This circumstance leads to the growth of the void. There are two more voids visible. One is located at the right end of the top interface and the other at the right end of the previously mentioned horizontal grain boundary segment. The growth at

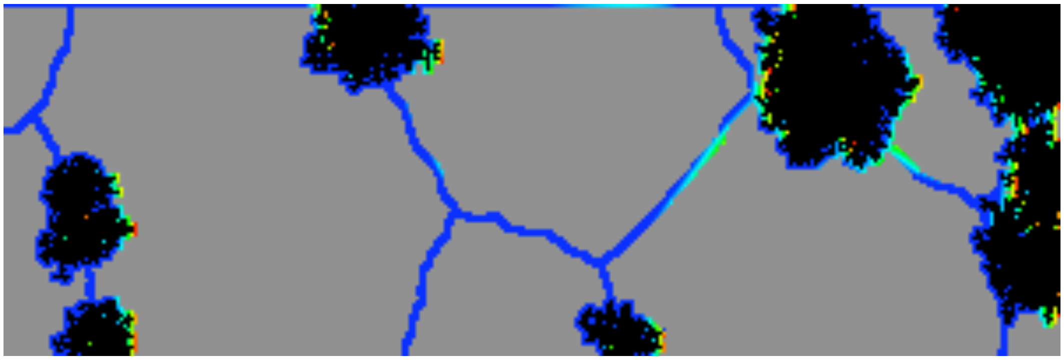
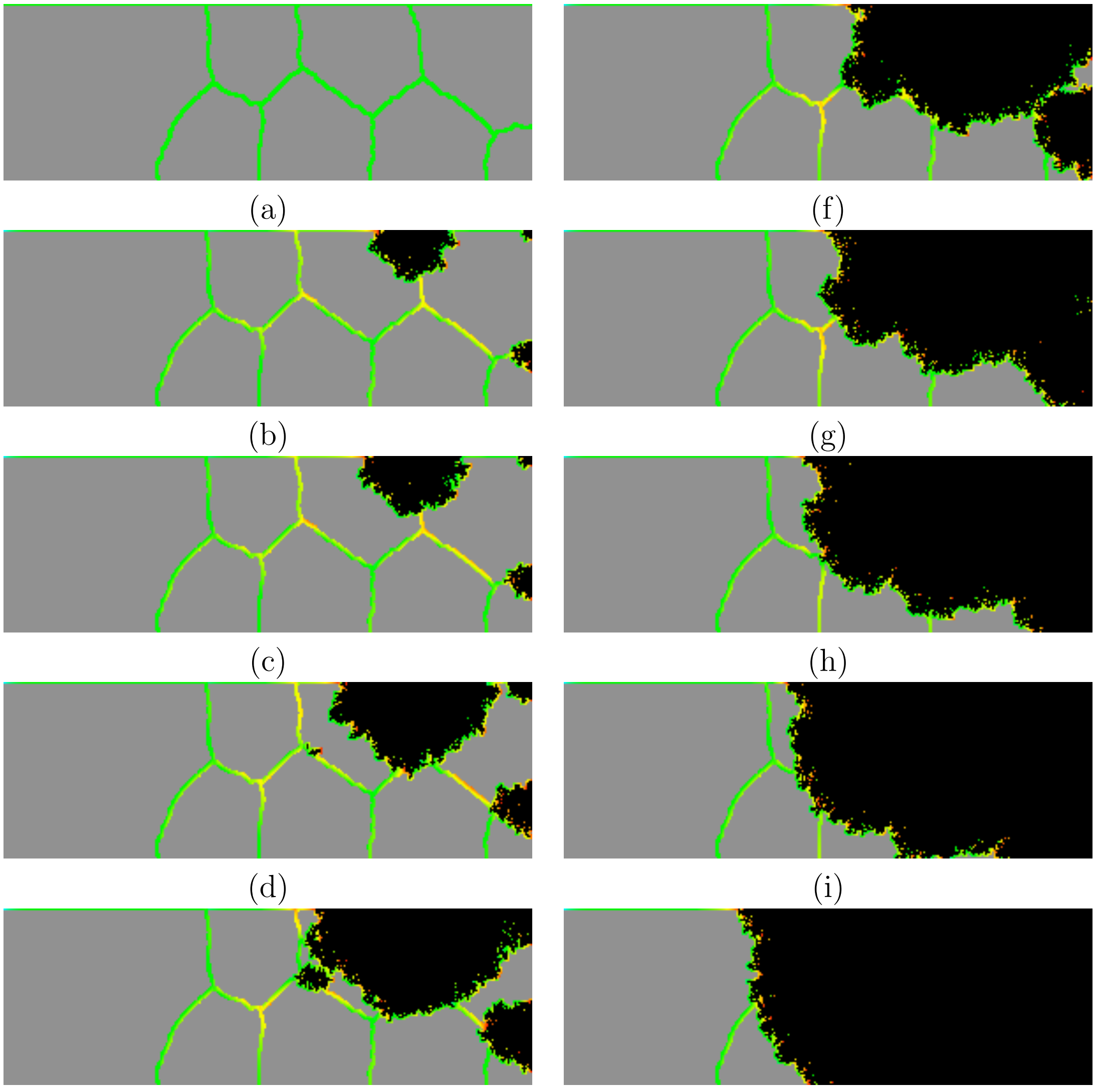


Figure 4.15: 100×300 nm^2 interconnect piece. As in Figure 4.14, but with applied void growth model ”Random/voidweighted”. The former long void at the top interface appears now centered as well.



(a) (f) (b) (g) (c) (h) (d) (i) (e) (j)

Figure 4.16: Void growth image sequence using the random-based void growth model. Electron flow is from the right side to the left side of the images. From a) to j) the void growth snapshots are shown at 1, 500, 715, 1430, 2146, 2861, 3576, 4291, 5007 and 6437 in units of 1000 computation steps, where one computation step converts to 30 ns.

both of these locations is also plausible because the right end of the image is a diffusion barrier, which means vacancies are transported towards the right end (the cathode end), but not away. Vacancies accumulate at the cathode end and the accumulation leads to void formation and growth. In Figure 4.16c, these three voids continued to grow larger. The grain boundary triple point at the center of the image (bottom of the middle one of the three upper vertical grain boundary segments) is orange, which means that vacancies start to accumulate also at this location. In particular, the vacancy flux at this location is more clear in Figure 4.5. In Figure 4.16d, the formation of a void is shown at this location (image center, bottom of the middle upper vertical grain boundary segment). All of these voids continue to grow as seen in 4.16e and coalesce in Figure 4.16f to for a final cathode void. This final void continues to grow until the end of the simulation in Figure 4.16j.

In summary, the voids start to form at three types of locations: grain boundary triple points, grain boundary-interface triple points and at the cathode end of interface and grain boundary segments. These locations are expected, plausible and agree with real interconnect electromigration damage sites [72]. In this section, several physically less reasonable void shapes have been presented. In order to create a more realistic void growth model that generates physically reasonable geometries, the energy of the void/solid surface has to be taken into account, which was not done in the simulation of this dissertation.

4.5 Summary

In this chapter, an introduction to electromigration was given and the most important electromigration simulation models were laid out. Starting from the empirical model to extrapolate electromigration lifetimes, the Black equation, electromigration simulation models like the Kirchheim and the Korhonen model were presented. Further, FEM and Monte Carlo simulation models were mentioned. Subsequently, the model used in this dissertation was discussed, which is based on a finite difference approach, using a forward-Euler technique to integrate the flux equation. The model was applied to simulate void nucleation and growth. The development of the void nucleation and growth algorithm was presented in chronological order, and an example of the final algorithm was given as a void growth image sequence. The final void growth algorithm, the random-based void growth, will be employed in the statistical simulations of the next chapter. The details of the simulation parameters and justification of the choice of simulation settings are provided in Chapter 6, the discussion chapter of this dissertation.

Chapter 5

Statistical Analysis

In the previous chapters it was described how the microstructure for the two-dimensional interconnect segments is derived and how the electromigration degradation is simulated while monitoring the electrical resistance. In this chapter, these algorithms are applied to large and statistically relevant sets of sample segments for statistical simulation. The lifetime for the individual samples per set is determined as described in Section 4.2.5.

The sets of interconnect segments were calculated on a parallel computer, the Dell Linux cluster Lonestar at the University of Texas at Austin, which was discussed in more detail in Section 2.2.2. Each individual segment of a set was calculated by one processor of the parallel computer in such a way that the whole set was computed simultaneously.

5.1 Setup Of The Sample Sets

In Tables 5.1 and 5.2 the setup of the sample sets is displayed. Overall, a number of 23 simulations were carried out on the parallel computer, each simulation operating on one set of samples. The samples within one set were identical except for the microstructure. The different microstructures were achieved by seeding the random number generator used by the Monte Carlo algorithm with a different number for each individual sample of a set. In order to ensure a unique seed for each of the samples, which is treated by one processor, the random seed is calculated as the sum of the master seed plus the identification number of the process computing the sample. The identification number of the processes can vary for example from 0 to 99 for a simulation incorporating 100 processors, meaning a set of 100 samples. The identification number is also called rank in the parallel computation. The master seeds are listed in Tables 5.1 and 5.2. The seeds were recorded in order to be able to retrace a simulation later if necessary. Note that the seed is also responsible for the distribution of random relative diffusion constants onto the grain boundaries and the top interface, as described in Section 4.2.1.

Set	n	length in nm	height in nm	CPU time in sec	Random seed	MCS	MGS in nm	D_N	D_{GB}	$\log(t_{50})$	σ
1	35	300	100	370639	18061956	2000	69	1-100	1-10	7.46	0.30
2	100	300	100	1144317	4081953	2000	69	1-100	1-10	7.57	0.36
3	100	300	100	2536252	4101979	2000	69	1-100	1-10	7.49	0.37
4	100	3000	100	8629246	5111983	2000	69	1-100	1-10	7.44	0.17
5	100	300	100	1367317	17535	2000	69	1-100	1-10	7.51	0.32
6	100	300	100	241571	22100901	1000	49	1-100	1-10	7.45	0.37
7	100	300	100	1514613	22100901	500	35	1-100	1-10	7.32	0.37
8	100	300	100	554857	22100901	500	35	1-10	1-10	8.02	0.24
9	100	300	100	1601281	22100901	1000	49	1-10	1-10	8.23	0.21
10	100	300	100	1094747	12082009	1000	49	51-150	1-10	6.57	0.67
11	100	300	100	1138872	12082009	300	27	51-150	1-10	6.73	0.56

Table 5.1: Setup and results of the statistical simulation. Part 1. The CPU times do not account for parallelism. An individual CPU time is the sum of all processor times. All significant numbers were kept to function as reference and identification number of a simulation set.

Set	n	length in nm	height in nm	CPU time in sec	Random seed	MCS	MGS in nm	D$_N$	D$_{GB}$	log(t$_{50}$)	σ
12	100	300	100	1359332	12242009	300	27	151-250	151-250	4.77	0.40
13	100	300	100	1143386	12242009	1000	49	151-250	151-250	5.60	0.45
14	100	300	100	1184706	1232010	1000	49	1-10	151-250	6.57	0.85
15	100	300	100	1091415	1242010	300	27	1-10	151-250	5.11	0.37
16	100	300	100	1266465	1252010	1000	49	1-10	15-24	7.07	0.26
17	100	300	100	1216668	1252010	300	27	1-10	15-24	7.78	0.37
18	100	300	100	1241962	1272010	500	35	151-250	51-150	5.61	0.38
19	100	300	100	1291700	1272010	1000	49	151-250	51-150	5.88	0.44
20	100	300	100	1360639	1282010	500	35	1-10	51-150	6.44	0.47
21	100	300	100	1257399	1282010	1000	49	1-10	51-150	7.01	0.60
22	100	300	100	1032048	1312010	500	35	401-500	51-150	5.15	0.28
23	100	300	100	1237214	1312010	1000	49	401-500	51-150	5.27	0.33

Table 5.2: Setup and results of the statistical simulation. Part 2.

The samples were almost all 300 nm and 100 nm in length and height, respectively. For the finite difference calculation this means that the samples were 300 rows in length and 100 columns in height, because the calibration was set to 1 nm per cell edge length. Only the samples of set 4 were 3 μm in length to see the effect of the interconnect segment length on the electromigration lifetime distribution. As will later in this chapter be shown in more detail, the lifetime distribution of the longer samples resulted in a much tighter sigma, e.g. 0.17 instead of 0.3-0.37.

The number of samples per set was chosen to be 100 for almost all of the sets. Only the first set was limited to 35 samples. This set was a first try to probe if the number of samples is sufficient for a good distribution. The lifetimes result is depicted in Figure 5.1. The course of the lifetimes distribution was not found to be very satisfactory. Especially the low percentiles were below the fit line and followed a line much steeper than the overall fit line. Therefore the number of samples per set was increased to 100. The result is shown in Figure 5.2, displaying the lifetimes distribution for set 2. It was found that this curve follows a log-normal distribution much better and from here on the number of samples per set was kept at 100.

For the rest 22 of the 23 sets, the mean grain size, the interface and grain boundary diffusivity was varied in order to study the effect of microstructure and top interface on electromigration lifetimes. In the first 5 sets the grain growth algorithm was run for 2000 Monte Carlo steps (MCS). According to Table 3.1, the mean grain size is 69 nm, keeping in mind that the edge length

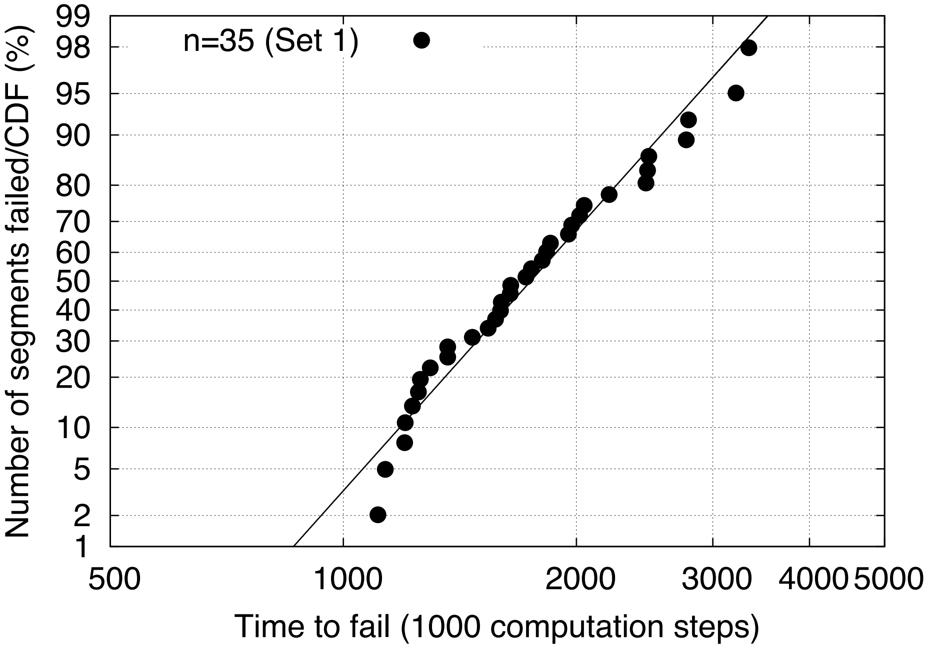


Figure 5.1: Lifetime distribution for set 1. The number of samples was set to n=35. For details see Table 5.1.

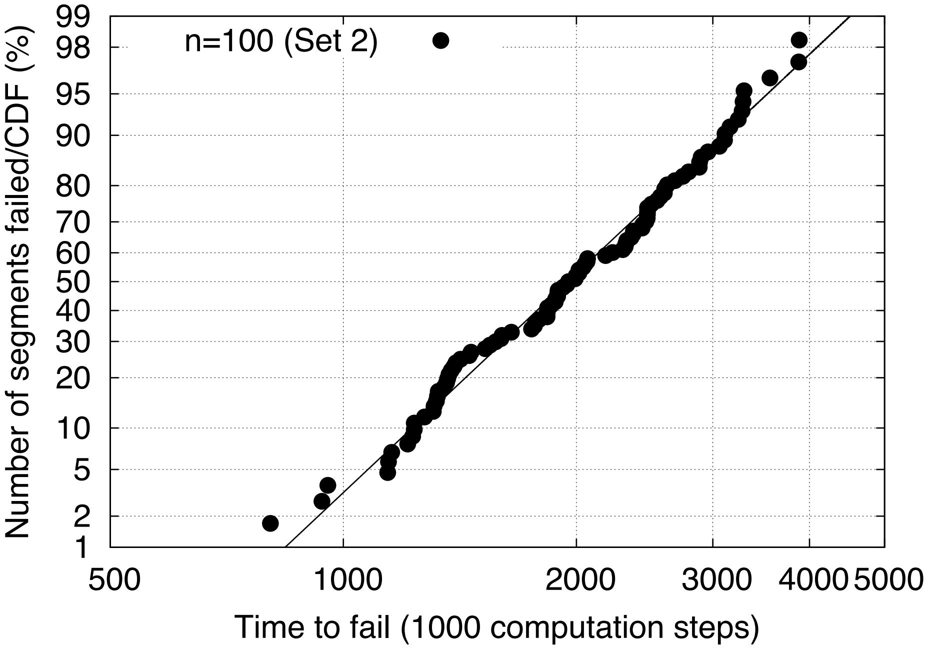


Figure 5.2: Lifetime distribution for set 2. The number of samples was set to n=100. For details see Table 5.1. The course of the distribution follows a log-normal fit much better compared to the distribution in Figure 5.1.

of one lattice site is 1 nm. The relative diffusivity for the grain boundaries was set in the range of 1 to 10 and for the top interface in the range of 1 to 100. The absolute diffusivity is calculated as the product of the base diffusivity D_{base} as listed in Table 4.2 times the relative diffusivity. This means that by average the diffusivity of the top interface is 10 times larger than the diffusivity of the grain boundaries, which corresponds to the top interface as the faster diffusion pathway.

For set 6 and 7 the mean grain size was decreased to 1000 MCS (49 nm) and 500 (35 nm), respectively, to see the effect of the grain size.

In set 8 and 9, in addition to varying the grain size between 1000 and 500 MCS, the relative diffusivity of the top interface was reduced to the range of 1 to 10, making the top interface as strong as the grain boundaries.

For set 10 and 11, the diffusivity of the top interface was increased to the range of 51 and 150 while setting the grain size to 1000 MCS and 300 MCS (27 nm).

In the following four sets (12-15), the grain boundary diffusivity was increased to 151-250 while varying the top interface diffusivity to ranges 151-250 and 1-10. This was done to see the effect of a top interface set much stronger than the grain boundaries. The grain size was varied between 1000 and 300 MCS, again, to also see the grain size effect.

The next two sets (16,17) correspond to the trial of reducing the grain boundary diffusivity to 15-24, which is still higher than the strong interface (1-10). The grain size was set to 1000 and 300 MCS.

In the last 6 sets (18-23), the experiment to study the grain size and top in-

terface effect was repeated for strong, intermediate and weak interface (1-10, 151-250 and 401-500 relative diffusivity, respectively) at a grain boundary diffusivity in the range of 51-150 and grain sizes of 1000 and 500 MCS.
In the following section the results of these experiments will be shown.

5.2 Results Of The Statistical Simulations

The results of the statistical simulations are depicted and described in the following sub-section. Each sub-section is about a specific sample set, studying the effects of grain size, interface strength and grain boundary diffusivity.

5.2.1 Line Length Effect

Figure 5.3 shows the results of set 2 through 5. The mean grain size was set to 2000 MCS (69 nm). All four sets show a similar median lifetime. The sigma except for set 4 is also comparable (0.32-0.37, according to Table 5.1). The sigma for set 4 is much smaller (0.17), where the segment line length was set to 3 μm.

5.2.2 Grain Size Effect

In Figure 5.4 the grain size effect is shown. Grain sizes were set to 500, 1000 and 2000 MCS, which corresponds to 35, 49 and 69 nm. Clearly all lifetimes for a given percentile are larger for the 49 nm than for the 35

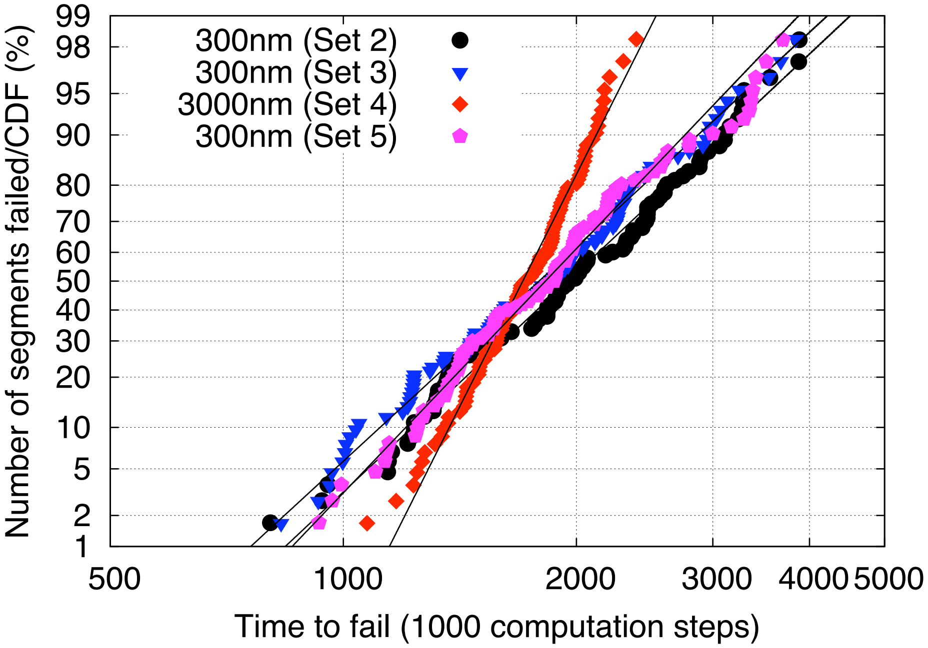


Figure 5.3: Lifetime distributions for set 2 through 5, showing similar median lifetime t_{50} and sigma for interconnect segment line length 300 nm and comparable median life time for the 3 μm case. The sigma of the latter case is much smaller.

nm mean grain size. At least half of the distribution (below 50% for a given percentile) of the 69 nm mean grain size is larger than for the 49 nm. The rest of the lifetimes distributions for 49 and 69 nm overlap, but the mean lifetime t_{50} for the 69 nm mean grain size is still larger. The sigma of the three sets is comparable (0.32-0.37). According to the logarithms of the mean lifetimes 7.32, 7.45 and 7.51 (see Table 5.1) for the mean grain sizes 35, 49 and 69 nm, respectively, the following dependence is suggested: a higher mean grain size leads to a larger electromigration lifetime.

5.2.3 Grain Size And Top Interface Effect

Figure 5.5 shows lifetimes distributions for a weak and strong top interface as well as for small and large grains. Here, weak and strong refer to ranges 1-100 and 1-10 of the relative diffusivity, respectively. Likewise refer small and large grains to 35 and 49 nm mean grain size. For both, the weak and the strong top interface (cap), the lifetimes increase for larger grain sizes, where the effect is more pronounced for the strong interface. Comparing weak and strong interface, the lifetimes increase significantly from $\log(t_{50})$ 7.32 and 7.45 to 8.02 and 8.23. The sigma decreases from 0.37 for the weak interface to 0.21 and 0.24 for the strong interface. The first observation is consistent with the previous sub-section, in the sense that larger grains lead to higher lifetimes. Here, this effect is more pronounced for the stronger interface, meaning that the influence of the microstructure almost diminishes for the weak interface. The second observation is that a strong interface leads to higher lifetimes,

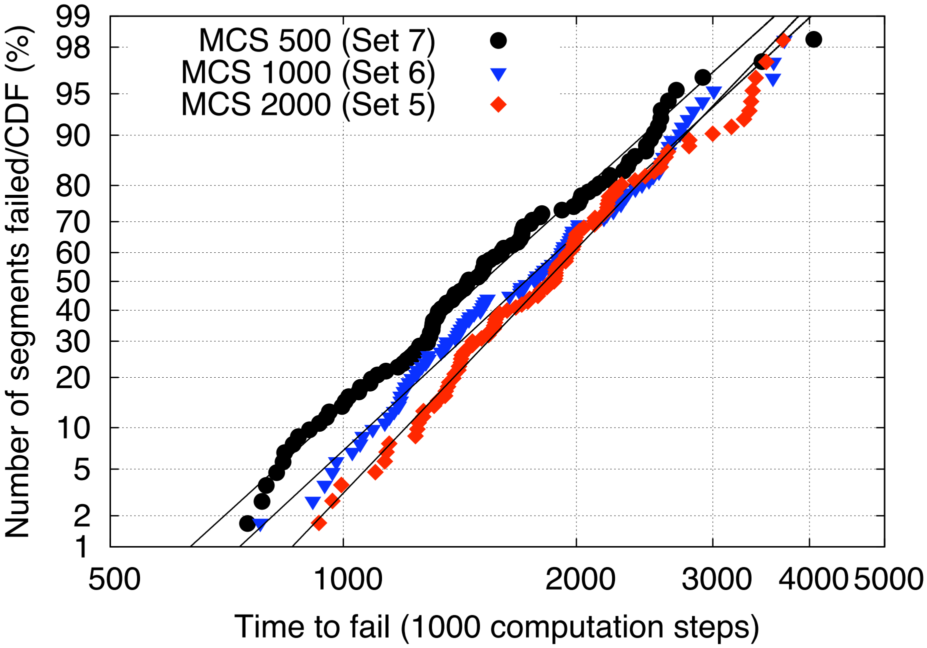


Figure 5.4: Grain size dependence of the lifetimes distribution. The MCS (Monte Carlo steps) refer to the mean grain size. 500, 1000 and 2000 MCS correspond to 35, 49 and 69 nm, respectively.

which is expected. The third observation is that the sigma decreases for the stronger interface.

For the results in Figure 5.6 the spread of the grain sizes was increased in such a way that 27 (small grains, SG) and 49 nm (large grains, LG) were treated. At the same time, the top interface was made much weaker (51-150 relative diffusivity range). The two distributions overlap for at least one third (percentile 70 and up) such that the distributions are not much different. So even for a larger spread in grain size and a weaker interface, the microstructure effect is not very pronounced, which is consistent with the observation in the previous paragraph.

5.2.4 Grain Size And Top Interface Effect Part 2

For the results of Figure 5.7 the experiment of sub-section 5.2.3 is repeated for much faster grain boundaries and the larger spread in grain size of 27 versus 49 nm. Here, fast grain boundaries refer to 151-250 relative diffusivity range. The weak interface was set to 151-250, which is the same as the grain boundaries, and the strong interface was set to 1-10, which is much lower than the grain boundaries. Some of the observations are the same as in the previous sub-section: larger grains lead to larger lifetimes and strong top interfaces lead to larger lifetimes as well. While the sigma for small grains and large grains is comparable for the weak interface (0.40 and 0.45), the sigma for large grains and strong interface is much higher (0.85) than the sigma for large grains and weak interface (0.37). This is inconsistent with the observa-

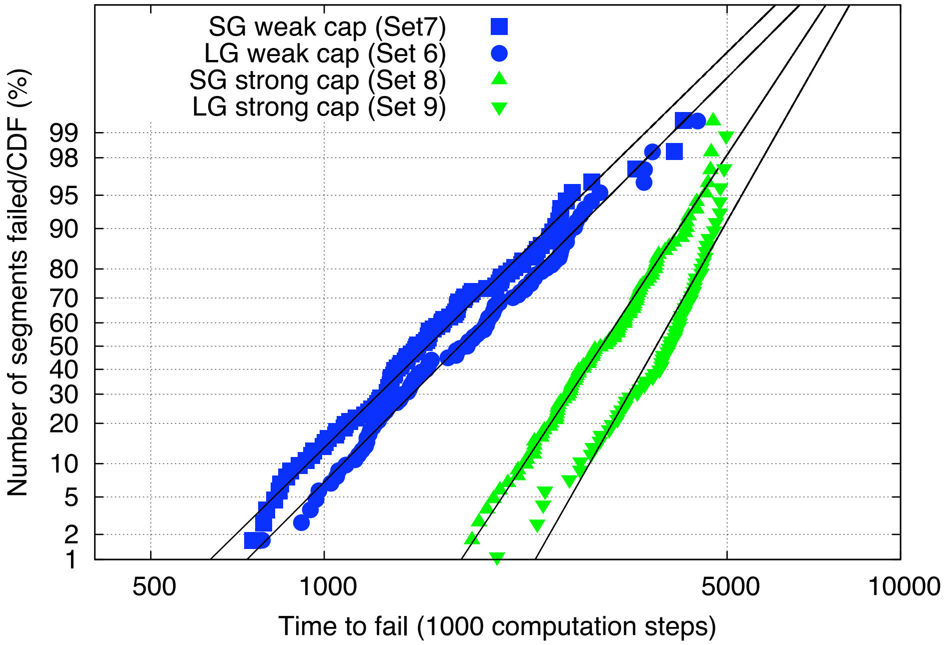


Figure 5.5: Lifetimes distribution behavior for small (SG) and large grains (LG) as well as weak and strong top interface (cap). Small grains refer to 35 nm mean grain size and large grains to 49 nm. The relative diffusivity of the weak interface is set to 1-100 and that of the strong interface to 1-10.

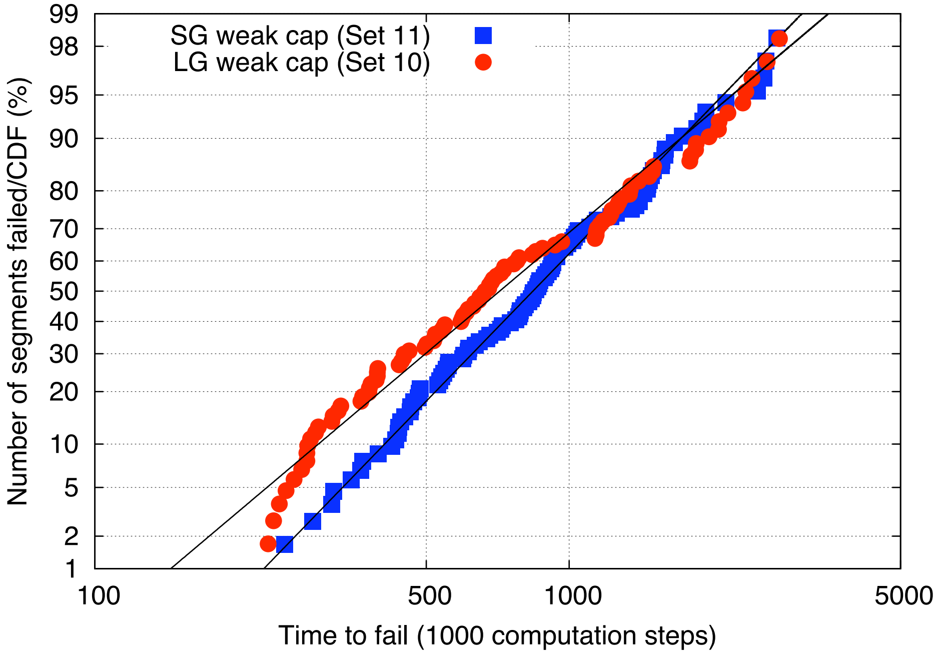


Figure 5.6: Grain size dependence of the lifetimes for a weak top interface. Small grains (SG) are set to 27 nm and large grains (LG) are set to 49 nm. The weak top interface (cap) means a relative diffusivity of 51-150.

tion of the previous sub-section, where the sigma decreased for large grains and strong interface. Another observation is that the increase in lifetime from weak to strong interface for the case of small grains is only minimal. In fact, the weak interface with large grains has higher lifetimes than the strong interface with small grains. It is to be noted that the weak interface diffusivity is in the same range as in that of the grain boundaries. For small grains it seems the top interface adds only minimally to the mass transport, since many diffusion paths are present when the grains are small. Since the top interface adds only minimally, it is to be expected that the effect of strengthening the top interface leads to an insignificant difference. Hence, the small grain-strong interface lifetimes are close to those of the small grain-weak interface case.

5.2.5 Grain Size And Fast Grain Boundary Effect

Figure 5.8 shows the results of the statistical simulation experiments for varying mean grain sizes while varying the relative diffusivity of the grain boundaries. Here, the interface is set strong for all four sets (1-10 relative diffusivity). Small and large grains refer, again, to 27 and 49 nm, respectively. Fast grain boundaries were set to 151-250 relative diffusivity and slow grain boundaries to 15-24 relative diffusivity.

One clear observation is as observed in the previous sub-sections that larger grains lead to higher lifetimes. With exception of the large grains-fast grain boundary case, one can observe generally smaller lifetimes for faster grain boundaries. The exception case large grains-fast grain boundary shows an

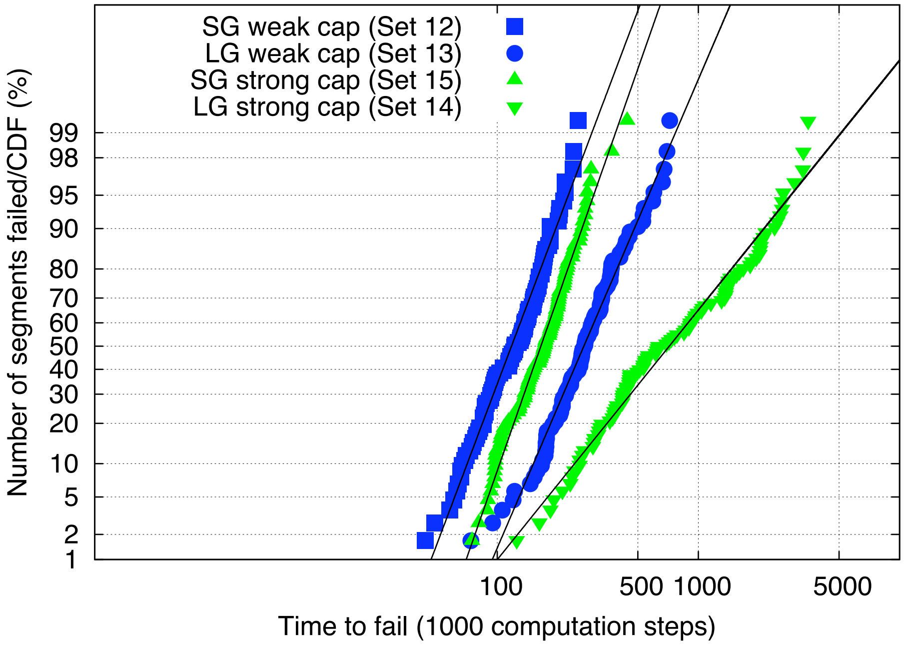


Figure 5.7: Grain size and interface strength dependence of the lifetimes distributions. Small grains (SG) refer to 27 nm mean grain size and large grains (LG) to 49 nm. Weak cap means 151-250 relative diffusivity for the top interface and strong cap means a relative diffusivity in the range of 1-10.

unusually high sigma (0.85) compared to all the others (0.26, 0.37 and 0.37). The lifetimes range from those seen in the small grain-fast grain boundary case for the low percentiles to those seen in the large grains-slow grain boundary case for the high percentiles, meaning that the lifetimes spread across the range of all the other distributions.

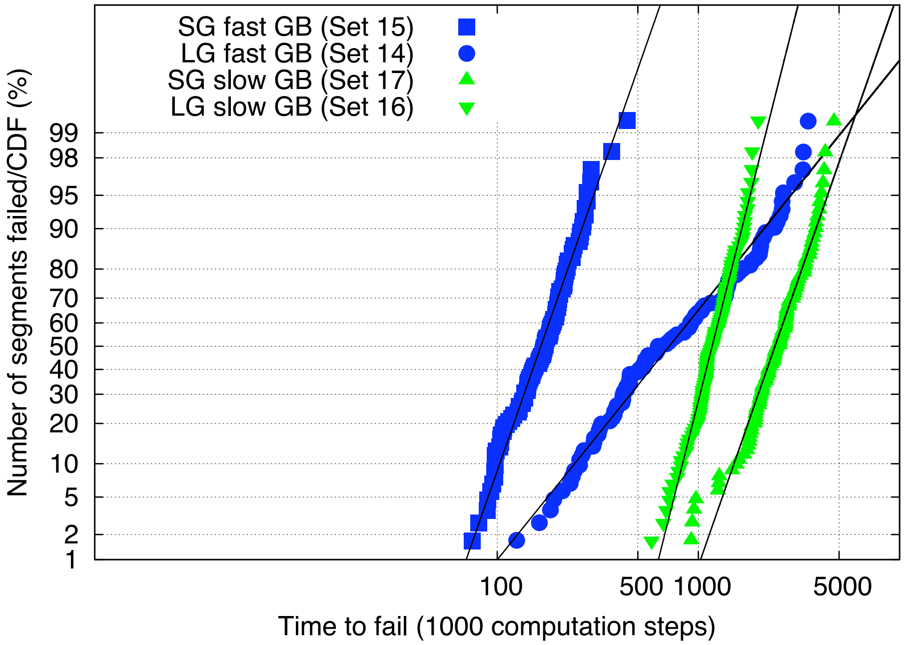


Figure 5.8: Grain size dependence of the lifetimes distributions for fast and slow grain boundaries. SG refers to small grains (27 nm) and LG to large grains (49 nm). The relative diffusivity of the fast grain boundaries is set to 151-250 and that of the slow grain boundaries to 15-24.

5.2.6 Grain Size And Top Interface Effect Part 3

Here, the simulations of the previous Grain-Size-And-Top-Interface-Effect Subsections is repeated for the case of fast grain boundaries and one additional very weak interface. The previously called weak cap is now called the intermediate cap and the very weak cap is the weak cap. Grain sizes were varied between 27 and 49 nm.

The consistent observation is that, again, larger grains lead to higher lifetimes. The second observation is that the intermediate cap has intermediate lifetimes between the weak and the strong cap, which was expected. The third observation is that the sigma increases steadily from the small grains-weak interface case (0.28) to the large grains-strong interface case (0.60). This is consistent with Subsection 5.2.4, but inconsistent with Subsection 5.2.3.

5.3 Summary

In this chapter, the algorithms for electromigration, void nucleation and growth from Chapter 4 were applied to statistically simulate the effects of microstructure and top interface on electromigration lifetimes. The simulated electromigration lifetimes follow a log-normal distribution, which is a justification of the implemented model, since log-normal distributions are generally observed in physical experiments. The term statistical particular means that the simulations were run for a large population (n=100) of interconnect segments to yield statistically relevant results. The major observation of the simulation results of this chapter is that electromigration lifetimes depend on

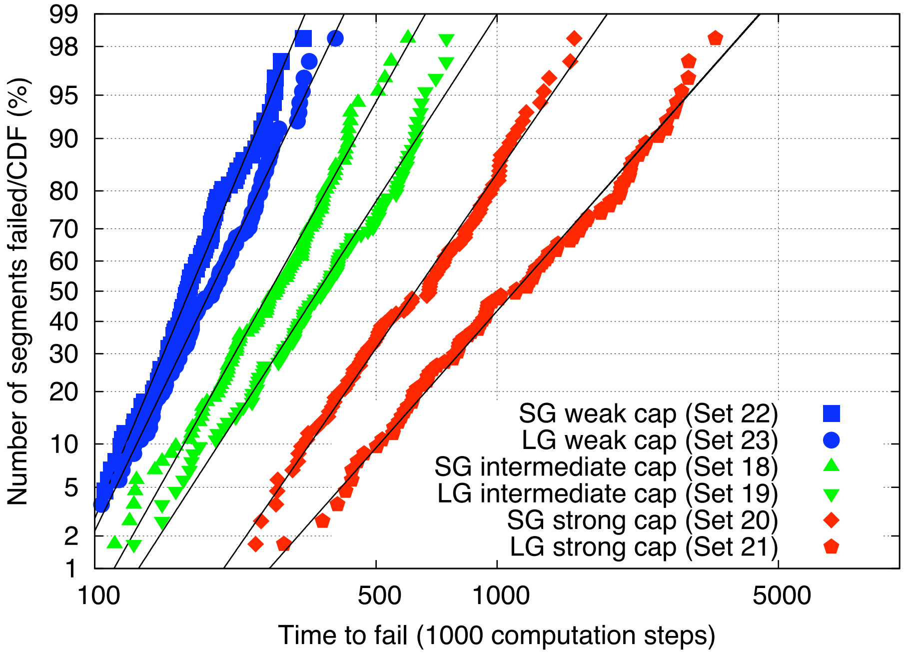


Figure 5.9: Grain size and interface strength dependence of the lifetimes distributions. SG refers to small grains (35 nm) and LG to large grains (49 nm). The ranges of the relative diffusivity for the weak, intermediate and strong interface is set to 401-500, 151-250 and 1-10, respectively.

the microstructure in such a way that large grains prolong the median time to fail. This observation is especially true for slow diffusing top interfaces. A discussion of the results and the simulation settings will follow in Chapter 6, the discussion chapter of this dissertation. There, a comparison between the simulation results of this dissertation and results from physical experiments will be included. Basically, the conclusion will be that the simulation results follow the trend of the results from physical experiments in a qualitative way. Due to the complexity of the task, the simulation development is not sufficient enough to allow a quantitative analysis.

Chapter 6

Discussion

6.1 Simulation settings and parameters

The development of the computer program in this work was aimed at simulating the electromigration phenomenon in a two-dimensional interconnect model segment. A finite difference method was employed to carry out the computation. The lattice was exclusively set to 100 cells in height and 300 cells in length. Other lattice geometries can be treated in future work to for instance study the geometry dependence of the lattice on the electromigration simulation results. The lattice geometry of 300×100 cells was chosen as a compromise between sufficient computation domain and computation time. The duration of an electromigration simulation with 5 million time steps takes approximately 3 hours. This duration was chosen as an acceptable limit between simulation runs and adjusting/developing the code. In 5 million time steps the depletion of material in the interconnect segment was approximately two thirds of the whole computation domain, which is well beyond the fail criteria of 400% percent electrical resistance increase.

The 400%, or five times the initial value, was chosen while observing the jumps of resistance increases of the individual resistance traces over computation time. It was observed that once a full height of material from the interconnect is depleted, the resistance jumps well passed the 400% mark for almost all traces, after having increased slowly and gradually. A depletion of the full height means that only the modeled Ta/TaN layer at the bottom of the interconnect carries the current at at least one cross-section of the interconnect. The chosen failure criterion differs from the 10%-criterion typically employed in physical experiments (sometimes a range of different failure criteria from 1% to 20% are applied, depending on the experiment [21]). This is because the modeled line is much shorter than physically tested lines. While a depletion of a full cross-section in physically tested lines that can be hundreds of micrometers in length causes only an electrical resistance increase in the low percents, e.g. 10%, the depletion of a full height in the modeled two-dimensional segments, which are 300 nm in length, causes a much higher relative resistance increase, well beyond the 10% mark. That is why a 400% fail criterion was chosen.

The calibration with physical units for the 300×100 cell domain was set to 1 nm per edge length of a cell. This seemingly arbitrary calibration is justified in the following way. The aim was to model polycrystalline lines in the dimension of 100 nm in height. The initial goal was to model 100 nm in width, which could not be done because of the two-dimensional nature of the simulation, meaning the interconnect segment is one cell edge length (1 nm) in width. The Monte Carlo (Potts model) algorithm was set to grow the grains in such a way that the line remains polycrystalline. Since the height in cells is 100 and the desired height in nm is 100, the calibration was set simply to one cell edge length to 1 nm in physical units.

The calibration in time is rather difficult. For the finite difference simulation a forward-Euler method was used. That means that the concentration of vacancies for the following time step in one cell was calculated as the sum of the current concentration plus the derivative multiplied by the duration of one time step. The derivative equals the flux divergence of the cell, that is the net flux divided by the length of the cell edge. The net flux is the difference in number of vacancies per cell face between what comes in left and at the bottom and what goes out at the top and at the right. The forward-Euler was chosen for simplicity reasons. As a counter part for the simplicity, the algorithm is very inefficient and very small time steps are needed for the calculation to be stable. In particular, time steps below the microsecond regime were applied. That means that for 5 million time steps, as were calculated for each simulation run, the total simulation time is less than one second. Certainly, no electromigration even under accelerated conditions would occur in that time frame. The time window for the diffusion by forward-Euler is one second, and the time window for electromigration under accelerated conditions is up to months. In order to work around this limitation, the current density in the simulation was set exorbitantly high: 10^{14} A/m^2. That equals 10000 MA/cm^2 and is four orders of magnitudes higher than the several MA/cm^2 used for physical testing with accelerated conditions. With this adjustment the time window of electromigration becomes comparable to the time window of the forward-Euler diffusion. One might argue that results produced with this parameter set is irrelevant. Later, it will be shown that simulation results do resemble the trend of physical testing, at least in a qualitative way. It is to be noted that the simulation does not take into account effects that would occur during physical testing at such high current density, for example heating and melting of the interconnect in the least. The high electric current density simply accelerates the electromigration process and catapults the degradation process into the one second time frame. Nevertheless, a time scale in the one second regime on an electromigration lifetime plot would be irritating and misleading. That is why the number of computation steps is kept as the time unit in the lifetime plots, etc. Without the high current density, the simulation of electromigration with the forward-Euler method would not be possible. Since the entire simulation is based on the forward-Euler method as the solver for the electromigration/diffusion equation, the high current density must be tolerated. A better approach for the future would be an implicit method (the forward-Euler is explicit) with an appropriate time step control technique. Though an implicit method can be less accurate, the algorithm is much more stable for longer time steps. When it will be possible to extend the diffusion time window to months instead of one second, then an adequate current density can be applied. The implementation of an implicit method will be left to future work.

As mentioned above, the forward-Euler method was used to solve the initial value problem of vacancy transport caused by diffusion and electromigration. The forward-Euler method is an explicit one-step technique. In terms of high stability, high efficiency and high accuracy, this technique is the least likely to be chosen. However, the forward-Euler method is the most intuitive approach to solve the initial value problem. This fact of intuitive approach was the reason why the method was decided upon to use it for the vacancy transport model. The term explicit means that for the time step to be calculated only past values of vacancy concentration are used. In contrary, for an implicit method, the next value in time depends on values of the same next time step, which are not readily available, such that a system of algebraic equations needs to be solved. The complexity is considerably higher compared to the forward-Euler method. However, the stability increases for the implicit method, which would allow larger steps in time. An example for an implicit method is the popular Crank-Nicolson technique [73]. The error of the forward-Euler method is of first order, which is less accurate than multi-step techniques, such as Runge-Kutta methods[1] [74]. Multi-step and implicit methods will not be further explored in the scope of this dissertation. Instead, it is referred to the References [73, 74]. Above all the advantages of multi-step and implicit schemes, the forward-Euler method was kept for it being the most intuitive and least complex approach.

The top row of cells of the computation domain was declared as the top interface. For convenience, only the top row was declared in such a way. That means that the interface is 1 nm in thickness. A similar thickness is true for

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[1] The simplest Runge-Kutta method is the forward-Euler technique, with only one stage/step.

the grain boundaries. From the qualitative crystallographic orientation map those cells that have at least one neighbor with different orientation were determined to belong to the grain boundary. At such a boundary, where grains A and B meet, the border line of cells of grain A and grain B, which individually are 1 nm in thickness, are counted as the grain boundary. That way the grain boundaries are effectively 2 nm thick. The limitation to 1 nm for the top interface and 2 nm for the grain boundaries was set initially in the beginning of the development of the simulation code to make the computation more convenient and to see qualitative results for the electrotransport of material. Then the limitation was kept throughout the end of the simulations in order to compare results. This limitation was tolerated because the high current density already permits only qualitative computations. In order for a more quantitative analysis, at least the grain boundaries will have to be set to less than 2 nm, which will possibly be done in future work.

As mentioned above, the calibration was set to 1 nm per cell edge length. If one chooses a different calibration, for instance when wanting a higher resolution for the simulation, the grain boundary and interface width will also change. In this simulation, only computation domains with 300×100 cells were treated, with one exception in Chapter 5, where the length was set to 3000 cells in length once. No other resolution was considered for experiments, because the used resolution was a good compromise between sufficient results and computation time. For future work it is absolutely necessary to decouple the grain boundary and the interface width from the resolution when one wants to study the effect of different resolutions. For example, when doubling the resolution to 600×200 cells computation domain while maintaining the size of 300×100 nm^2, the interface width would halve to 0.5 nm and the grain boundary width to 1 nm. An algorithm must be developed that includes the appropriate number of cells for the interface and the grain boundaries. One possibility could have been to use a finite element mesh to make such distinction, but that would have increased the complexity of the electromigration simulation dramatically. The change in complexity would have been so high that the effort to make the interface and grain boundary cell distinction would have been out of proportion compared to the rest of the simulation. The focus of the dissertation was to produce EM statistics results in reasonable amount of time, and the implementation of a finite element mesh would have expanded that time frame drastically. The implementation of a finite element mesh could definitely be a proposal for future work.

As driving force for the material transport, only the electromigration driving force was included in the simulation. In that sense the computation is similar to the diffusion path approach for electromigration simulation. The methods for electromigration simulation are classified into the three groups: diffusion path approach, driving force approach and other models [15]. The diffusion path approach is characterized in one way as only regarding the electromigration driving force. The model in this work does not regard mechanical stress gradient induced migration, temperature gradient induced migration or surface tension induced migration. An attempt was made to include the stress gradient induced driving force, but the forward-Euler algorithm was not stable. After some effort, the intention to include stress migration was surrendered and only the electromigration driving force was taken into account for the simulation. This way the electromigration simulation program could be termed inadequate, because the impact of stress migration and thermal migration is just as high, meaning the ratios of these driving forces over the electromigration driving force are about 1 [15]. Nevertheless, the motivation remains that what difference one can see in the electromigration results for different microstructures. The simulation results are still meaningful, because they reflect the trend of observations from physical experiments in a qualitative way (Figure 6.1). When a possible implicit method replaces the forward-Euler technique and the implicit method ensures stability, the intention of implementing stress migration can be reenacted in the future.

Since electromigration is the only implemented driving force, phenomena like the short-length-effect (Blech-effect) or stress-induced voiding cannot be observed with the simulation presented in this work, because these phenomena are based on the stress migration driving force. Since there is no short-length-effect, the vacancy transport due to electromigration is not counteracted by an opposite vacancy transport caused by stress build-up. The vacancy flow does not cause a stress build-up, because stress is not implemented in the model. Therefore, vacancy transport caused by electromigration continues without the counterbalance of an opposite stress migration flow. There is no critical length of the interconnect segment, or a critical current density, or a combined critical length-current-density-product $(\mathrm{jL})_c$, below which electromigration degradation does not occur due to a dynamical equilibrium of electromigration and stress migration as in real interconnects. The consequence of neglecting stress migration on electromigration lifetimes is not clear. On the one hand, the electromigration lifetimes can be overestimated by the simulation, because vacancy transport caused by electromigration is not retarded by an opposite stress migration flow. On the other hand, electromigration lifetimes can as well be underestimated, because a certain stress state inherited from an annealing process of the interconnect can as well cause stress migration in the direction of electromigration vacancy transport. Additionally, stress-induced voiding does not occur in the simulation, which could also decrease the lifetime of the interconnect.

The question is how relevant are the results of the simulation while neglecting the effects of stress migration. It is not clear whether missing stress migration changes the results qualitatively or just in a quantitative way. One way to support the notion that it does not change the results in a qualitative way is the fact that a comparison with physically obtained experimental data and simulation data shows the same trend (Figure 6.1). To what extend the results of the simulation are affected in a quantitative way can not be further investigated with the means of the simulation presented in this work. It is not obvious that the quantitative differences in the lifetime improvement between physical and simulation experiment in Figure 6.1 is mainly due to the fact that the simulation neglects stress migration. The simulation can only make a prediction of the electromigration lifetimes of interconnect segments when electromigration is the only driving force.

As mentioned above, the electromigration driving force is solely responsible for the vacancy transport. Initially, each cell of the computation domain, which typically consists of 300×100 cells, is filled with 20 at.% vacancies. This number was taken from Kirchheim's model [44], where electromigration in aluminum interconnects was treated. Kirchheim himself stated that this number of 20 at.% is unreasonably high, but was chosen to yield sufficient stresses in a reasonable amount of computation time. The same applies here - the number was chosen to yield voiding in a reasonable amount of computation time for the copper interconnect segments. With an atomic volume of 10^{-5} m^3/mol and, therefore, a number of 10^5 mol/m^3, the vacancy concentration was set to 20,000 mol/m^3. When the vacancies are transported and redeposited through electromigration, the vacancy concentration may eventually reach 30,000 mol/m^3 at sites of positive vacancy flux divergence. This number of 30,000 mol/m^3 was chosen as the threshold for void nucleation for the experiments described in Chapter 5. In case that the site of flux divergence is truly a void nucleation site, meaning that no neighbor site is void yet, an index is switched for the cell indicating that it is now a void cell. The value of 30,000 was obtained empirically, testing different values from 20,000 to 100,000 mol/m^3 and it was found that 30,000 yielded voiding in a reasonable amount of computation time. In actuality, the cell would be void at 100,000 mol/m^3, because the vacancy concentration would then be at 100 at.%, but because of diffusion, the number of 100,000 was never reached in the simulation. This fact lead to the decision to use a lower number than 100 at.%, and 30 at.% proved to be reasonable for voiding in less amount of computation time. On the flip side, looking at copper instead of vacancies, 70 at.% of copper atoms are still inside the cell when the index is changed indicating that the cell is void. This means the cell is not really empty when declared void, and the material is lost to the simulation. The disappearance of material is tolerated, otherwise void nucleation would not be possible in this model.

The question is how the voids should grow. In the beginning there was the idea that void could grow in the same way they are nucleated, meaning that once the vacancy threshold of 30,000 mol/m^3 is reached, the index is flipped and the cell is declared void. This approach didn't work because of the formation of zig-zag artifacts as shown in Section 4.4 and Figure 4.9. Instead, the conclusion was made to use a random-based void growth algorithm as described in Section 4.2.3.1. In this algorithm, when a cell reaches the vacancy concentration threshold of 30,000 mol/m^3, and a neighboring cell[2] is void already, then the following procedure is applied. Firstly, the entire cluster of contiguous void cells is determined if there is more than one connected void cell. Secondly the surface cells of the cluster are determined. Thirdly, one of the surface cells is chosen at random. This surface cell is the cell whose index is flipped and which is declared void, not the original cell that reached

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[2] one of the nearest neighbors left, right, top and bottom or one of the second nearest neighbors (the diagonal ones)

the threshold. Following this procedure, the void grows in a circular fashion, which is the main reason why the conclusion was made to use this void growth algorithm.

The voids grow irreversibly, are stationary and do not virtually move. These facts are due to the limitation of the void growth algorithm - it does not allow the redeposition of material. In physical experiments, voids usually nucleate and grow somewhere along the length of the interconnect. If the top interface is not strengthened, then the voids appear normally at the top interface and usually at a grain boundary. After void formation and continuing electromigration, material is depleted at the upstream end of the void and redeposited at the downstream end of the void. That way the surface of the void shifts upstream and the void seems to move towards the cathode end of the interconnect (upstream). This movement is called virtual movement, because the void does not actually move. It is the material that is redeposited downstream. The simulation does not handle this kind of downstream redeposition of material and there is no virtual movement of voids in the simulation. The voids stay where they are nucleated and only grow larger. No observation can be made that voids virtually move towards the cathode end and accumulate in one big cathode void as in real interconnects. A replacement of the random-based void growth algorithm, which also handles virtual movement of voids, is a possibility for future work.

While the voids grow, the electrical resistance needs to be monitored. The algorithm used for calculating the resistance of the interconnect with voids is described in Section 4.2.4. It was decided to use the simple slice model. In this model, each column of cells of the computation domain is one slice. The column is extended by an additional cell at the bottom, which corresponds to a Ta-based shunt layer. For each slice, the non-void cells are counted. The non-void cells are treated as if they were contiguous, which in general they are not. Further, the non-void cells plus the additional shunt cell are viewed as parallel resistors and the electrical resistance of the slice is calculated accordingly. The resistance of the entire interconnect segment is calculated as serial connection of the slice resistances. This procedure has a substantial advantage - it delivers a quick and simple measure for the resistance of the interconnect segment. The disadvantage is that this procedure can underestimate the electrical resistance. Non-void cells per slice are treated contiguously. Isolated non-void cells that would not contribute to conduction will be counted as conducting cells in this algorithm. Also, the current density is not uniform in real interconnects. Besides the fact that non-uniform current density is not treated in this simulation, one can assume that downstream cells next to a void will not contribute to conduction. A model to mask out these non-conducting void cells was developed by Noack [75]. In his bachelor thesis, Noack elaborately discusses the modeling of on-chip interconnect resistance calculation, including the simple slice model. Besides the existence of improved models, it was decided to keep the simple slice model as the method of resistance calculation because of its more intuitive access to understanding.

With the ability for void nucleation, growth, electrical resistance monitoring and failure determination, it is possible for the simulation to predict the lifetime of an interconnect segment for a given microstructure configuration. The goal of this dissertation was to be able to do statistical simulations of the effect of microstructure on electromigration lifetimes. The simulation experiments were laid out in Chapter 5. For the microstructure generation, a Monte Carlo technique based on the modified Potts model was employed. The results of the Potts model closely resemble the properties of polycrystal microstructure, as described in Section 3.1. It is possible to control the mean grain size of the interconnect segment by the number of Monte Carlo steps (MCS), as shown in Table 3.1. However, it is not possible to control the standard deviation sigma of the grain size distribution. This is a significant disadvantage of the Potts model, where the sigma increases steadily with MCS. It is a disadvantage, because this approach does not allow the investigation of the grain size distribution sigma on the electromigration lifetime distribution sigma. This kind of investigation would be very interesting, because although the origin of the log-normal distribution of electromigration lifetimes is not well understood so far, it is believed that the log-normal distribution of the lifetimes is caused by the log-normal distribution of the grain sizes. Ceric and Selberherr [22] use a Finite Element Method (FEM) approach for the statistical simulation of electromigration lifetimes, and their microstructure generation tool is capable of producing grain size distributions with desired standard deviation. In future work, it will be interesting to exchange the microstructure generation algorithm with that of Ceric and Selberherr in order to study the coupling of grain size distribution and electromigration lifetime distribution sigma.

6.2 Simulation results

The first observation of the statistical simulations laid out in Chapter 5 was that a longer line length leads to a smaller lifetime distribution sigma (0.17 compared to 0.32-0.37, Figure 5.3), whereas the median lifetime t_{50} is about the same. The reason for the comparable median lifetime could be that only one void spanning the whole height of the interconnect segment is necessary to fail it. There is an equal chance that such a void would grow in the long as well as in the short segments. If no other nucleation site is to be found, such a void would grow for sure at the cathode end, because the cathode end is a diffusion barrier. The void growth at the cathode end is approximately independent of the line length. The growth only depends on the vacancy flux of the top interface, which should be the same for the long as well as for the short segments. The sigma for the long lines is probably smaller due to the fact that the long lines provide many more nucleation sites than the short ones. Hence, many more growing voids compete to fail the long segments, keeping in mind that only one height-spanning void is enough to fail the segment. It is to be expected that the distribution of lifetimes is tighter (smaller sigma) when many voids compete to fail the segment than a smaller number of voids. Therefore, the sigma decreases for longer segments.

The second major observation from the statistical simulations was that large grains prolong the lifetimes of the interconnect segments, especially for the case of a strong interface. A strong interface means that the diffusivity range is comparable to the diffusivity range of the grain boundaries. The reason why the grain size effect is not as pronounced for a weak interface (diffusivity range much higher than for the grain boundaries) is clearly that most of the vacancy transport happens along the top interface and not along the grain boundaries. Therefore, only little vacancy transport is contributed by the grain boundaries, where only a small effect of the grain size is to be expected. The reason for the grain size effect could be the fact that overall there are more grain boundaries present for small grains. This means that more fast diffusion pathways exist for the case of small grains. More diffusion leads to a decrease in lifetime. On the flip side, when the grains are larger, less fast diffusion pathways exist, limiting the overall diffusion and the lifetime increases.

With the statistical simulations of Chapter 5, modeling the effect of microstructure, the goal of this dissertation has been reached. What is left to do, and most importantly, is a comparison of the results with actual physical experiments on real interconnects. Figure 6.1 displays the results of physical experiments [2] in comparison with some results of this dissertation. What is shown is the outcome for four different cases: small (SG) and large grains (LG) combined with strong (with CoWP coating) and weak (without CoWP coating) top interface. The weak interface refers to a conventional SiCN capping layer. For the LG structure, the average grain sizes was 215 nm at the trench top and 181 nm at the trench bottom. The SG structure showed 123 nm average grain size at the trench top and 126 nm at the trench bottom. Hence, the SG structure had significantly smaller grains than the LG structure. The physical test structures consisted of interconnects with 72 nm in depth (width), 144 nm in height and 200 μm in length (compared to 100 nm in height and 300 nm in length for the simulation, which is two-dimensional). The physical electromigration test was performed at 300 °C and at a current density of 1.03 MA/cm^2. The simulation plot is a reproduction of sets 20-23 from Chapter 5. All four cases from the physical experiment and the simulation show the same trend. The shortest lifetimes can be observed for the SG/weak interface structures for the physical experiment as well as for the simulation. The highest lifetimes are shown for the LG/strong interface case. The grain size effect is only minimal for the weak interface - 2× lifetime improvement for the physical experiment and 1.1× improvement for the simulation. What is drastically different is the quantitative improvement for the strong interface. Here, for the physical experiment a 24× improvement for the SG structure and even a more than 100× improvement for the LG structure from weak to strong interface can be observed. Analogous in the simulation an improvement is found in the same direction, however, it is only 4× and 6× for the SG and LG structures, respectively. Even though physical experiment and simulation show the same trend, work needs to be done to improve the simulation in order for a more quantitative analysis. It is not clear why the improvements from weak to strong interface are so drastically different between physical experiment and simulation. First of all, the simulation with a total of 5 million time steps is not sensitive enough in order to allow a lifetime improvement of more than 100×. A median lifetime of 200,000 time steps for the weak interfaces in the simulation (Figure 6.1) would require at least 20 million time steps. Even then, such long lifetimes were never observed in the simulation. The reason could possibly be the fact that no material is redeposited in the simulation. When a void nucleates, it grows steadily until it spans the height of the interconnect segment and fails the line. Redeposition of material would prolong the lifetime, which is not implemented. The implementation of a redeposition-void-growth algorithm has already been discussed for future work.

A last observation that is similar for the physical experiment and the simulation is that the sigma increases from weak to strong interface and from SG to LG structure. For the simulation it can be stated that the sigma increases from small to large grains, probably because the sigma in the grain size distribution increases caused by the Potts model. Why the sigma increases from weak to strong interface in the simulation is not clear. Also, little information is available about the reason for the increasing sigma in the physical experiment.

Lastly, a comment follows about 3-dimensional calculations. The intention in the beginning of the dissertation was to make the calculations 3-dimensional. This development plan has been met for the grain growth simulation only. It turned out to be much more complex to turn the electromigration simulation into 3 dimensions than anticipated. This circumstance is mainly due to the fact that diffusion on surfaces of 3-dimensional grains is not as straight forward as diffusion on boundary lines of 2-dimensional grains. The impact of the increased complexity was such that a limitation to two dimensions for the electromigration simulation had to be made.

6.3 Summary

After the comparison between physical and simulation experiments, the chapter concludes with a review of the dissertation statements from the introductory Chapter 1, as these set the frame of this dissertation. The dissertation statements are listed again as follows:

1. The computer program developed in this work simulates electromigration reasonably well for a two-dimensional interconnect segment.
2. The model for electromigration simulation developed in this work can predict where material will be depleted, i.e. where voids nucleate in an interconnect segment.
3. The program simulates the growth of voids reasonably well.
4. The simulated electromigration lifetimes follow a log-normal distribution
5. The simulation reflects qualitatively the trend of the effect of small and large grains, as well as strong and weak top interfaces, which is consistent with physical experiments.
6. The software can be used for quantitative analysis.

For statement 1 can be said that the program simulates electromigration reasonably well, because of the fact that physical and simulation experiments show the same trend (Figure 6.1). For statement 2, voids in real interconnects nucleate at triple points[3], at the cathode end and at points where a grain boundary meets the top interface. All three of the void nucleation sites can be observed in the simulation experiment as well (Figure 4.16), which is why statement 2 is assumed to be true. Statement 3 is only true with the limitation that voids in the simulation do not virtually move. The redeposition of material is not implemented. Accepting the fact that voids are stationary and grow irreversibly, the void growth is modeled reasonably well. Statement 4 can easily be answered looking at all the Figures in Chapter 5: yes, the simulated electromigration lifetimes follow a log-normal distribution. Statement 5 was the conclusion of the previous paragraphs, where physical and simulation experiments were compared. The simulation reflects the trend of the physical experiment for the four cases: large and small grains combined with weak and strong top interface. Finally, the last statement must be answered negatively. The program presented in this work can not be used for quantitative analysis. In order to make the program more suitable for quantitative simulations, a number of improvements must be made, which have already been proposed for future work. Firstly, the width of the top interface and the grain boundaries must be adjusted appropriately. Currently, due to computational convenience, the interface and grain boundaries were set to be 1 and 2 nm in

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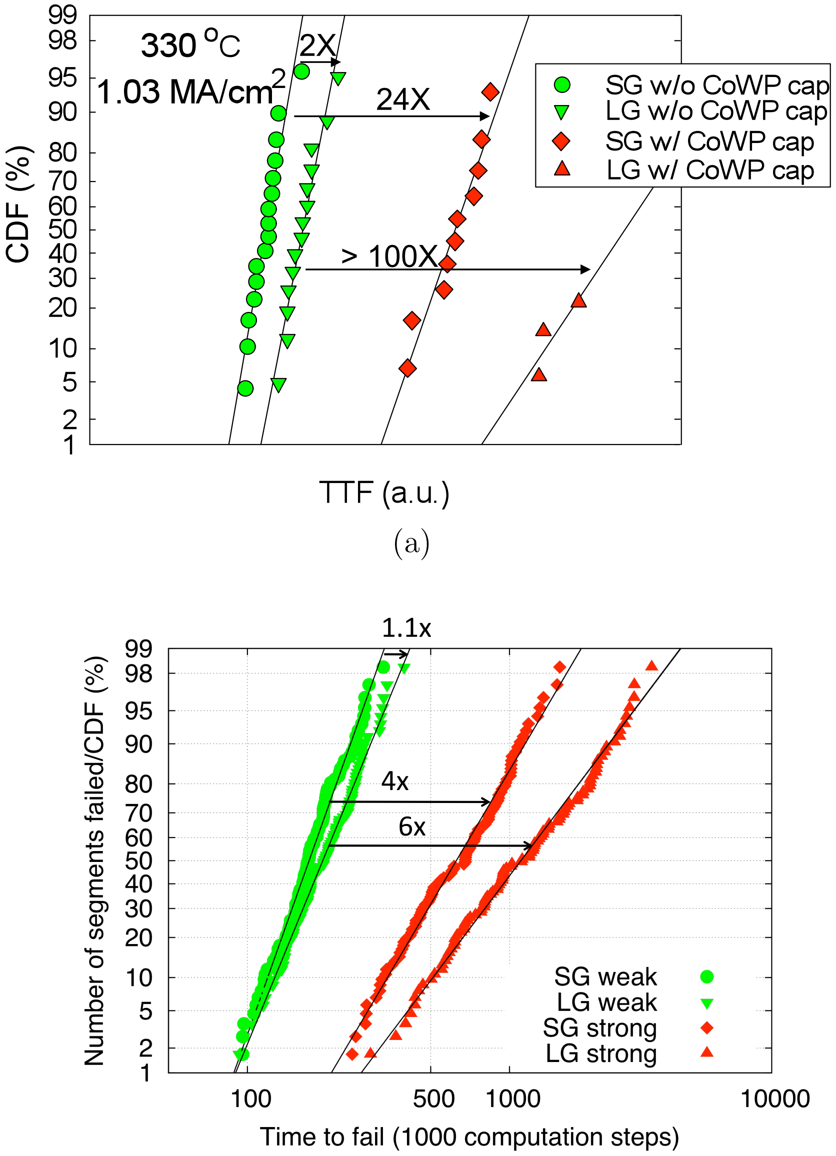
[3] points where three grain boundaries meet

width, respectively. A better algorithm should be implemented that sets the width at least for the grain boundaries to less than 2 nm. Further, a more efficient algorithm to solve the initial value problem of the vacancy transport should replace the forward-Euler method, possibly an implicit technique with a suitable time step control. This implementation would allow longer time steps that could actually cover hours instead of seconds. Then the current density can be adjusted to a more reasonable value, which is currently set to 10^{14} A/m^2 (10,000 MA/cm^2). With these requirements, quantitative analysis can be attempted. Thus far, the program is not suited for quantitative simulations.



(a)

(b)

Figure 6.1: Comparison of experimental and simulation results: (a) Experimental results [2]. (b) Simulation results of this dissertation.

Chapter 7

Summary and Future Work

7.1 Summary

The goal of this dissertation was to statistically simulate the effects of microstructure on electromigration lifetimes for on-chip copper interconnect segments. This goal has been reached with a variety of 23 sets of simulation runs, each set containing a population of mostly 100 segments. The computation was carried out on a parallel computer, the Dell Linux Cluster Lonestar of the Texas Advanced Computing Center (TACC) of the University of Texas at Austin. The segments of each population were simulated at the same time on the parallel computer, reducing the computation time from 300 hours down to 3 hours per set. The segments were two-dimensional, mostly 300 cells in length and 100 cells in height. The calibration was set to 1 nm per cell edge length, such that the interconnect segments were 300×100 nm^2 in spatial dimensions. The microstructures for each segment were generated with a Monte Carlo technique based on the modified Potts model with a number of Q=30 for different qualitative crystallographic orientations. The transport of vacancies was modeled along the grain boundaries and along the top interface. In the simulation, the interface and grain boundary thickness were set to 1 and 2 nm, respectively. The one-step explicit forward-Euler method has been employed to solve the initial value problem of the vacancy transport caused by electromigration and diffusion. Electromigration was the only driving force in the model. The electric current density was chosen unreasonably high (10^4 MA/cm^2), because the forward-Euler technique only allowed a simulation in the second time window, instead of hours. The diffusivities of the grain boundary network and the top interface were applied randomly, in multiples of a base diffusivity D$_{base}$. A different diffusivity was applied for each grain boundary and interface segment, each of these segments were sides of grains. The different diffusivities ensured the existence of vacancy flux divergent sites. When the threshold of 30 at.% vacancy concentration was reached in a cell, an index was flipped and the cell was declared void - a void nucleation. Initially, the vacancy concentration was set to 20 at.%. For the voids to grow, a random-based algorithm was used. The cell, by which the void will grow, is chosen randomly from the void surface, ensuring a circular growth. When the voids grow, the interconnect segment electrical resistance increases. The resistance was calculated with the simple slice model, adding the non-void cells of a column of the computation domain as parallel resistors and adding the column resistances as series resistances. Each column was extended by one cell representing a Ta-based shunt layer. A failure criterion of 400% was chosen, which is considerably higher than typical 10% for physical experiments, because the interconnects in the simulation are much shorter. With these requirements, statistical simulations were carried out. The grain size was varied between 27, 35, 49 and 69 nm, corresponding to 300, 500, 1000 and 2000 Monte Carlo steps.

The ratio of grain boundaries and interface diffusivity was modeled between 1:1, 1:10 and 1:50. A weak interface was modeled with a low ratio and a strong interface with a high ratio. The simulation showed that larger grains prolong the electromigration lifetimes, especially for strong interfaces. A comparison was made with the results of physical experiments. Both the simulation and physical experiments showed the same trends. The lifetime improvements of large grains and strong interfaces showed qualitatively the same properties, but not in a quantitative way. For example, the lifetime improvement with an additional CoWP coating in the physical experiment was more than 100× for large grains. Correspondingly, the lifetime improvement for a strong interface in the simulation was only 6×. Some future work is necessary in order to make the simulation program more suitable for quantitative analysis.

Table 7.1 provides an overview of the implemented and not yet implemented physics and features of the model. The table can help to plan future work.

7.2 Future Work

A major change for future work is the replacement of the one-step explicit forward-Euler method to solve the initial value problem of the vacancy transport. The forward-Euler technique was used for its intuitive access, but is not well suited in terms of accuracy, stability and efficiency. An implicit method with an appropriate time step control would be a better fit. Since the forward-Euler method is unstable for larger time steps, only a time window of seconds could be covered by the simulation. To still see an electromigration

Physics or feature	Implemented	Note
Diffusion in EM simulation	yes	
EM driving force in EM simulation	yes	
Stress gradient driving force in EM simulation	no	Will lead to critical line lengths and more accurate lifetimes
Volume and surface energy in the Potts model	no	Will simulate other driving forces than the curvature driven growth, would allow cute angles of grain boundaries with computational domain and prevent concave shapes, can simulate small grains mixing with large grains
Energy of the void/solid surface in the void growth algorithm	no	Would lead to more realistic void shapes
Implicit method with appropriate time-step control	no	The forward-Euler method must be replaced
Decouple grain boundary width from resolution	no	

Table 7.1: Overview of the implemented and not yet implemented physics or features in the model.

effect, the electric current density was set unreasonably high (10^4 A/cm^2). A more efficient and stable finite difference method, such as the Crank-Nicolson technique, could be able to cover hours of a time window that would allow a more reasonable current density (1 MA/cm^2). This is important for a more quantitative analysis.

Further, the finite difference problem should be stated in matrix formalism. Thus far, the cells of the computation domain were accessed by a loop, which is intuitive but not fast. If the problem is stated in matrix formalism, which means that the vacancy concentration of the cells of the computation domain will be put in a vector and multiplied by a matrix in order to differentiate it, highly optimized standard algorithms could be used to solve the matrix equation, such as BLAS (Basic Linear Algebra Subprograms) [76]. A simple test was done in Matlab [77], where a comparison between looping through cells and matrix multiplication was conducted. The matrix multiplication showed an acceleration of factor 4. This could be a promising approach.

So far, electromigration was the only driving force implemented in the model. In the future, stress migration should be included, because by magnitude it has the same effect as electromigration. When stress migration is included, phenomena like the short-length-effect (Blech effect) or stress-induced voiding can be observed in the simulation.

For computational convenience, the widths of the top interface and the grain boundaries have been set to 1 and 2 nm, respectively. The algorithm that determines the top interface and the grain boundaries must be improved to allow more real widths of less than 2 nm, at least for the grain boundaries. Also, the width of the grain boundaries and the top interface should be decoupled from the resolution, such that a doubling in resolution does not result in a halving of the widths.

In the simulation, mainly a computation domain of 300×100 cells was used. Once, the length was set to 3000 cells, and it was found that the electromigration deviation sigma decreased drastically for the longer interconnect segment length. It could be interesting to study the lattice size effects on simulation results further.

The modified Potts model used to generate the microstructures does not permit a control of the standard deviation sigma of the grain size distribution. Such a feature would be interesting to study how the grain size distribution sigma affects the electromigration lifetime distribution sigma. A possible candidate could be the microstructure generation tool used by Ceric and Selberherr [22].

The grain growth algorithm does not account for surface effects. As interconnect dimensions shrink, the surface to volume ratio increases, and surface effects become more pronounced. The general Hamiltonian for the Potts model allows the specific setting of a surface energy, which was not done in this dissertation, and could be done in future work. The surface energy is higher than the volume energy, and thus more small grains are expected in the vicinity of the surface, which limit the overall grain growth. An implementation of the surface energy has been done in the dissertation by Zhang [78]. It could also be possible to import real microstructures, for example from electron backscatter diffraction (EBSD) measurements.

The void growth algorithm does not allow redeposition of material. The voids grow stationary and irreversibly. Virtual movement of voids can not be observed. An improvement on the void growth algorithm should be made that eventually allows the redeposition of material.

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Vita

Matthias Kraatz was born in Schwerin, Germany on 17 July 1976, the first son of Hans-Joachim Kraatz and Rosemarie Kraatz. He received the Diplom-Physiker degree from the Brandenburg University of Technology in Germany in 2003. He applied to the University of Texas for the enrollment in their Materials Science program. He was accepted and started graduate studies in August, 2003. Due to personal reasons he needed to relocate to Germany in 2006 where he resumed studies at the Brandenburg University of Technology in the group of Professor Schmeißer in 2007 while remaining a registered student at the University of Texas.

Permanent address: Falkenweg 17
03130 Spremberg
Germany

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